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Pulse-width Modulation Techniques in Two-level Voltage Source Inverters – State of the Art and Future Perspectives

Research paper

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Abstract: The core of most power electronic systems involving DC/AC conversion is a voltage source inverter (VSI) that runs on some pulse-width modulation (PWM) strategy. Numerous PWM techniques have been reported in the literature over the past few decades, each having its own merits and limitations. This paper reviews some selected areas of two-level PWM VSI, namely proper utilisation of the DC bus without deteriorating the quality of the output waveform, switching-loss reduction in the linear and over-modulation zones, common-mode voltage and PWM strategies for its reduction or elimination, distortion of the output voltage owing to dead time, and its compensation. These phenomena are explained in brief, followed by discussions on different research works relevant to these areas, and their advantages and disadvantages. Finally, the paper shows prospective directions in which research may continue in these areas in future.

Keywords: *carrier-based PWM • common-mode voltage • DC-bus utilisation • space-vector PWM • dead-time distortion*

1. Introduction

Voltage source inverters (VSIs) have extensive applications in the fields of motor drives, utility interface in power systems, and uninterruptible power supplies for generating AC voltage outputs, whose magnitude and frequency can be controlled using various techniques such as delta modulation (Rahman et al., 1987), sigma-delta modulation (Bose, 2002), pulse-density modulation (Fujita and Akagi, 1996), pulse-amplitude modulation (Taniguchi and Okumura, 1993), pulse-width modulation (PWM) (Bose, 2002) etc. This paper starts its discussion with some of the topologies and modulation techniques associated with VSI, but mainly focusses on different two-level PWM techniques in VSIs. PWM inverters were first reported in literature by Schounung (1964). A three-phase two-level inverter, consisting of IGBT switches, is shown in Figure 1, where an equivalent three-phase star-connected load is assumed to be connected to the inverter. Extensive research is being carried out on PWM inverter topology, control, and application for the past few decades. This includes single-phase and three-phase as well as two-level and multi-level inverters. PWM techniques for inverters can be broadly classified into carrier-based PWM (CBPWM) technique and carrier-free PWM technique. Space-vector based PWM (SVPWM) technique, which was reported around the 1980s and 1990s (Boys and Handley, 1989; Handley and Boys, 1990; Holtz, 1992; Van Der Broeck et al., 1988), is the most popular among all the carrier-free PWM techniques. A detailed discussion on SVPWM has been given in Bose (2002).

Sine PWM (SPWM) technique is the most common type of CBPWM. In this technique, PWM pulses are generated by comparing a low-frequency modulating waveform, sinusoidal in shape, with a high-frequency triangular carrier wave. The principle is shown in Figure 2. In linear zone of operation, the maximum RMS value of

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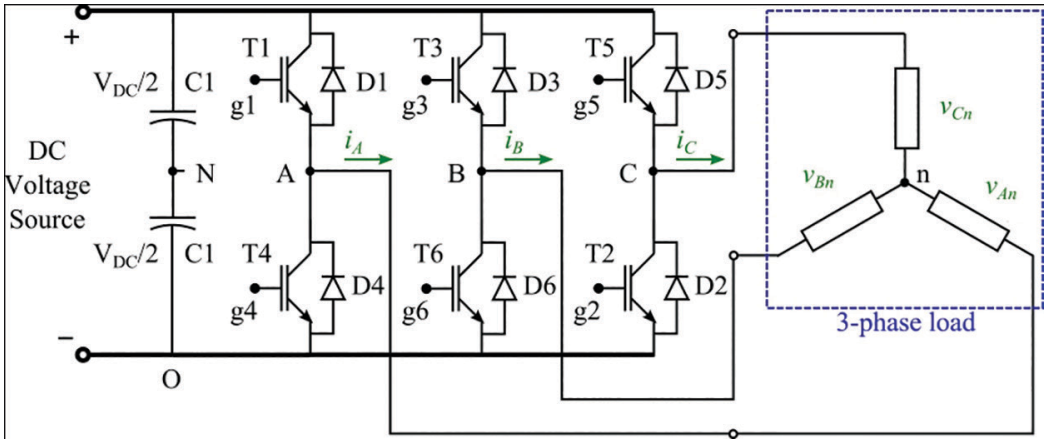


Fig. 1. Three- phase two-level inverter.

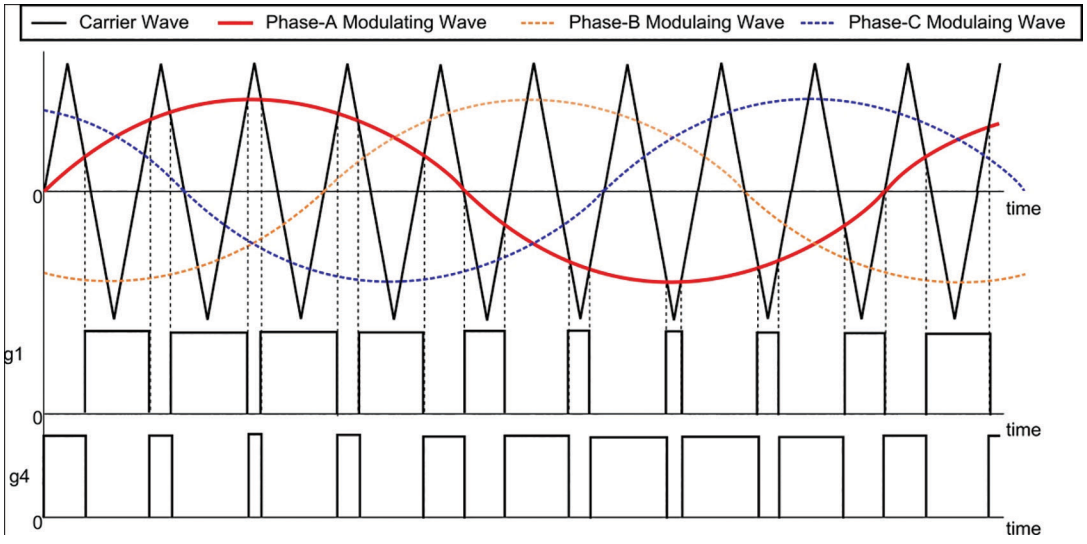


Fig. 2. Principle of sine-triangle PWM; modulating and carrier waves (top); gate- pulses g1 for switch T1 (middle) and g4 for switch T4 (bottom) via comparison of the carrier and phase A modulating waveforms; gate-pulses for the other switches of the inverter in Figure 1 can be generated by similar logic using the modulating waveforms of phases B and C.

output line-to-line voltage of SPWM inverters is only about 61.2% of the input DC voltage. Injection of suitable third-harmonic component to the modulating signal helps to increase the gain of the inverter by about 15.5% (Figure 3). Beyond this, the inverter enters into the over-modulation zone, resulting in further increase in gain, at the cost of introduction of lower-order harmonics in the output voltage, which are difficult to attenuate.

SVPWM is another approach, where direct determination of switch duty ratios is done by using the concept of voltage space vector in a three-phase system (Handley et al., 1990; Holtz, 1992). The principle of this technique is represented in brief in Figure 4. Here, the time for which the gate pulses of the upper switches of three inverter legs remain on within one switching cycle for sector-I and sector-II of the space-vector hexagon are represented in Figures 4a and 4b, respectively, whereas the generation of reference vector in different sectors of this hexagon is shown in Figure 4c. This magnitude of this reference vector depends on the on-duration of different switches, generating different active and zero vectors. This technique inherently achieves about 70.7% gain, while remaining in the linear zone. The performance in terms of inverter gain in SVPWM mode is fairly the same as compared to third-harmonic injected SPWM inverters. Entering the over-modulation zone in SVPWM mode results in the re-appearance of lower-order harmonics, just as in the case of CBPWM inverters. More effective utilisation of DC-bus voltage as compared to conventional SPWM, absence of high-frequency carriers and the associated synchronisation problems, optimum harmonic content for a wide range of load etc. are few of the advantages of SVPWM.

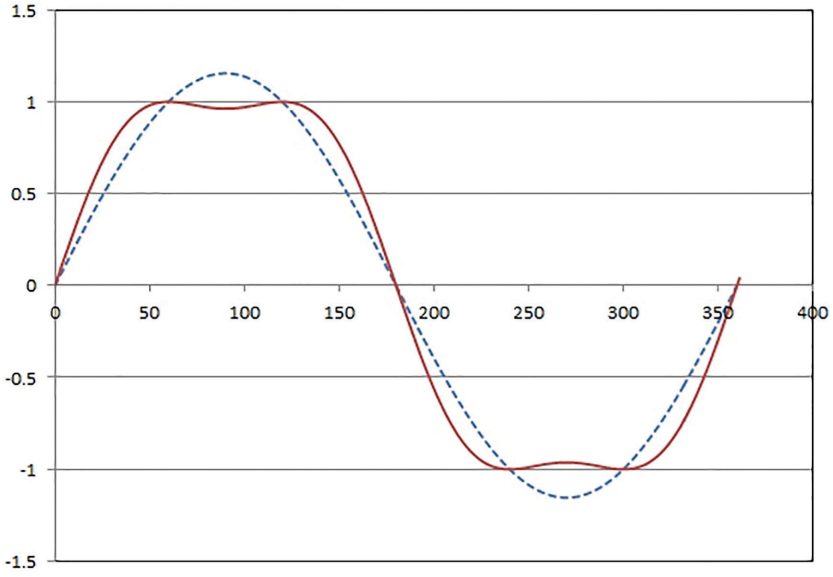


Fig. 3. Principle of third-harmonic injected sine-triangle PWM; Y-axis: modulating waveform (red) and its fundamental component (blue); scale: Y-axis: 0.5 unit/div, X-axis: 50°/div.

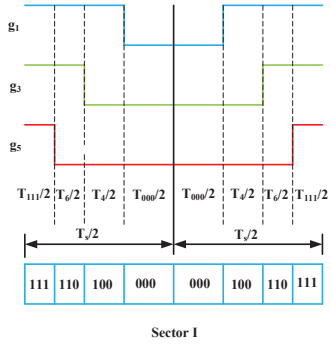
In the linear zone of operation of SVPWM, the output voltage fundamental component amplitude is a linear function of the amplitude modulation index of the inverter. Over-modulation region can be divided into two regions. In over-modulation region I, the trajectory is modified, such that for some time it follows a circular path with a radius higher than the reference magnitude and for the remaining time in the sector it moves along the boundary of space-vector hexagon. In over-modulation region-II, the modified trajectory totally follows space-vector-hexagon boundary (Chatterjee and Dalapati, 2020; Pal and Dalapati, 2012).

Numerous studies in the literature are available that try to address the problems of PWM inverters, by proposing modified PWM strategies and/or changes in inverter topology. Often it is observed that a proposed strategy brings in improvement in one of the problem areas but deteriorates the inverter performance from the aspect of another problem area. Hence, the search for an all-round-improved PWM strategy continues. This paper reviews some selected areas of two-level PWM VSI, namely (a) proper DC-bus utilisation and improvement of waveform quality, (b) switching-loss reduction, (c) common-mode voltage (CMV) reduction, and (d) dead-time distortion and its compensation. It discusses the merits and shortcomings of some of the solutions presented in the above areas. Based on these discussions, the paper comments on the overall progress in these areas and points towards the possible directions of future research in such areas.

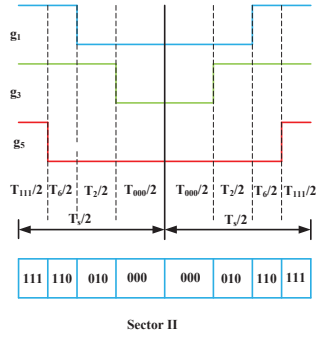
The remainder of this paper is organised as follows. Sections 2 discusses different PWM techniques and their advantages and shortcomings in the selected areas mentioned above; Section 3 provides the future scope of work in this area, as emerging from the discussion formulated in this paper; and Section 4 draws the conclusion.

2. Different PWM Techniques: Progress and Challenges in Selected Areas

Pulse-width-modulation based two-level VSI forms the heart of most power electronic systems in which DC/AC conversion is required. Numerous examples of such systems are available, such as grid-connected solar inverters, battery-driven vehicles, uninterruptible power supplies etc. SVPWM was developed as a vector approach to three-phase PWM inverters. This technique extends the linear modulation range of operation over conventional SPWM and provides much flexibility in PWM pulse-train generation. Here, numerical simulation has been done in MATLAB Simulink platform to show its performance in different operating regions. The basic block diagram representation of this simulation has been given in Fig. A1. It has been proved that SVPWM is equivalent in functionality to double-sided uniform-sampled PWM (UPWM) (Kwasinski et al., 2003), with the flexibility of splitting the null-vector intervals arbitrarily between V0 and V7. This relationship between two-level SVPWM and CBPWM has eventually led to



(a)



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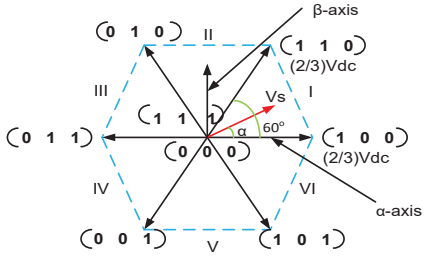


(c)

Fig. 4. (a) Principle of two-level SVPWM as applicable to the inverter of Figure 1. Logic for generation of gate pulses of the switches of upper legs for sector-I of space-vector hexagon (1 → on and 0 → off). (b) Logic for generation of gate pulses of the switches of upper legs for sector-II of space-vector hexagon (1 → on and 0 → off). (c) Reference vector generation in different sectors of space-vector hexagon (1 → upper switch on and 0 → upper switch off for three-phase legs).

the development of various PWM modulators (Fang et al., 2014). Although both of the above two types of PWM inverters have been generally accepted as controllable AC sources in almost all applications, there are several problems of inverters, controlled by these techniques.

Scope of Review

Over the past few decades, numerous research works have been undertaken around the world to improve several aspects of PWM techniques in two-level VSI. These research works focus on a wide variety of aspects of these PWM techniques. However, this paper focusses on the following aspects:

- Proper utilisation of the DC bus without affecting output waveform quality
- Switching-loss reduction in linear and over-modulation zones of PWM inverter
- CMV aspects and PWM strategies reducing it
- Reduction of output voltage distortion owing to the dead-time effect

Different research works relevant to these topics are discussed briefly in the forthcoming content comprised in this section. It may be noted that the above-mentioned areas are not totally isolated but are interrelated to each other, so that any improvement in one of the above areas may affect one or more of the others.

2.1. Proper utilisation of the DC bus without affecting output waveform quality

For a given input DC voltage, normal PWM inverters have a limited gain without entering into the over-modulation zone. Generally, operation in over-modulation zone is undesirable, as such operation causes lower-order harmonics to appear. Hence, under normal conditions, all inverters operate in under-modulation zone. Now, PWM inverters often have to work with sources wherein the input voltage may droop within a range (e.g. an array of lead-acid cells). In such cases, to ensure that the required output voltage is obtained even at the minimum input DC voltage, it is desirable to improve the inverter gain. This may be achieved by operating the inverter in the over-modulation zone, with subsequent increase in lower-order harmonics.

Numerical simulation has been done in MATLAB Simulink digital simulation platform to show the DC-bus utilisation in conventional SVPWM technique based three-phase two-level inverter in different operating regions. Here, linear operating region is specified by $0 \leq m_a \leq 0.866$, whereas over-modulation zones I and II are defined by $0.866 < m_a \leq 0.9091$ and $0.9091 < m_a \leq 1$, respectively, m_a being the amplitude modulation index, measured with respect to two-thirds of the DC-bus voltage. Some of the performance parameters of SVPWM based inverter have also been compared with those of conventional SPWM based inverter in a linear region. In this simulation, DC-bus voltage is taken as 560 V, inverter output fundamental frequency is 50 Hz, switching frequency is 6 kHz, and amplitude modulation index m_a for SVPWM are 0.8227, 0.873, and 0.95 for linear, over-modulation-I, and over-modulation-II regions, respectively, measured with respect to two-thirds of DC-bus voltage, whereas its value for SPWM in the linear region is taken as 0.95, measured with respect to semi-DC-bus voltage. The simulations have been performed with and without dead time, where the dead time is ascertained as 4 μs. The load resistance and inductance per phase are 10 Ω and 50 mH, respectively. The plot of the magnitudes of the fundamental component, as well as some of the lower and higher integral harmonic components, of the inverter output line voltage with frequency are shown in Figures 5 and 6.

From Figure 5, it can be stated that the magnitude of the fundamental component of the inverter output line voltage in the linear region is higher in SVPWM technique, as compared to SPWM technique. The magnitude of the fundamental component of the inverter output voltage increases when over-modulation regions of SVPWM technique are entered, the magnitude being highest in over-modulation region-II. This is shown in Figure 6.

Over the last few decades, intensive research studies have been carried out for increasing the utilisation of the DC bus of the inverter, maintaining the lower-order harmonic content within limits. Some of the strategies involve

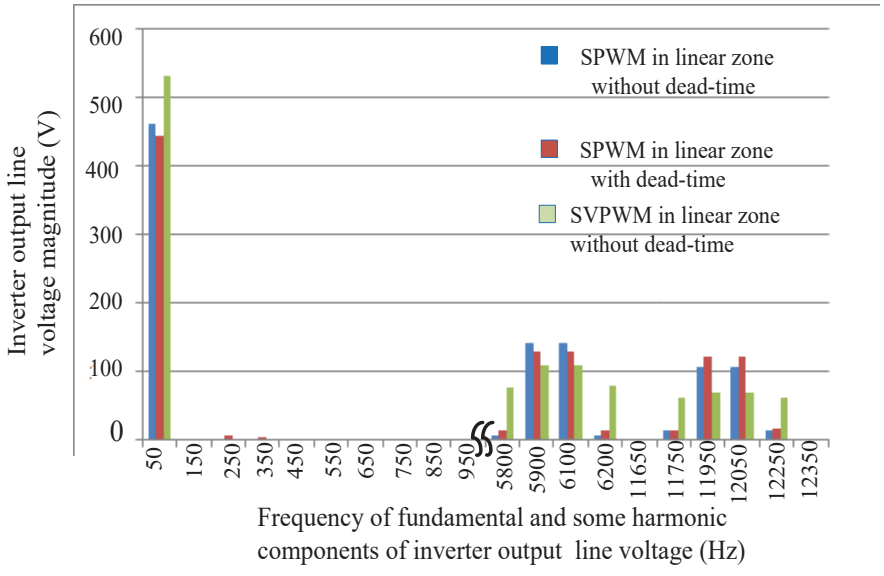


Fig. 5. Plot of the magnitude of the fundamental and some harmonic components of the inverter output voltage (V) with frequency (Hz) in the linear operating region of SPWM technique with and without dead time and SVPWM technique without dead time.

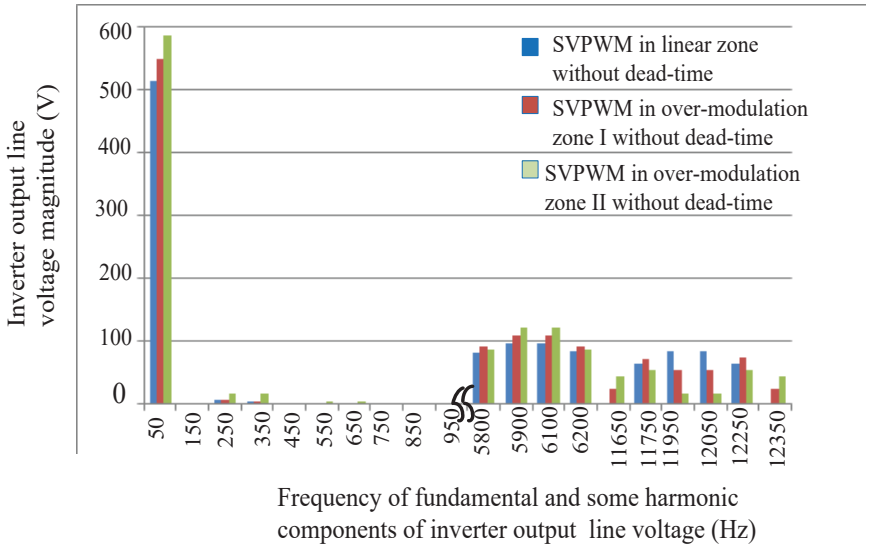


Fig. 6. Plot of the magnitude of the fundamental and some harmonic components of the inverter output voltage (V) with frequency (Hz) in linear, over-modulation-I, and over-modulation-II operating regions of SVPWM technique without dead time.

SVPWM technique, whereas some others involve CBPWM technique. However, while different works are able to address one or more particular objective(s), they may show a deterioration in another performance parameter or may increase the complexity or cost of implementation. Improved versions have also been reported as solutions to the problems of the previous ones, but with these are characterised by their own pros and cons. Some of the research works in this area are discussed below, including their basic idea and/or objective(s).

Several research works have been carried out for smooth transition from the inverter linear operating region to the six-step mode of operation. Different techniques have been developed involving inverter modelling, Fourier series expansion or reference and holding angles etc. For increasing the output voltage up to six-step mode in a continuously controllable manner, two different techniques have been proposed in Holtz et al. (1993). Here, for high dynamic performance with high-switching-frequency drives, a space-vector strategy is used, where distorted-continuous and distorted-discontinuous reference signals are used in over-modulation modes I and II, respectively. On the other hand, in high-power inverters having low switching frequency, a field-oriented PWM technique is applied. However, it involves an on-the-spot switching between the two over-modulation modes within a restricted output voltage range. Transition region characteristics for a number of modulation strategies are introduced in Kerkman et al. (1996). A compensated modulation technique (CMT), with continuous and discontinuous modulators, is applied for smooth transition to six-step operation and to eliminate the voltage error. To develop the CMT, for linearizing the inverter with any form of the modulating signal, an inverter-gain model of the PWM inverter throughout this transition region is used. In this technique, lower-order harmonics have not been addressed properly for the six-step operation. Also, the dynamic behaviour of the current controller on the voltage limit boundary has not been addressed. A square wave, set as a function of the modulation index, is added to each of the phase voltage commands in the pulse-dropping region (Kaura and Blasko, 1996). This technique extends the PWM linearity to the six-step mode of operation and also maintains the gain of the voltage fundamental component without reducing the dynamic range. The technique is demonstrated first for open-loop and then for closed-loop schemes. For the closed-loop scheme, the modulation index value is extracted from two current regulators. Here, there is a change in modulation index from one sample period to the next, which affects the square wave shape.

The research of Lee and Lee (1997) aims to improve the closed-loop regulation of the PWM inverter for achieving good dynamic response. Here, a novel over-modulation strategy, working on Fourier series representation of reference voltage, is discussed for SVPWM inverters. The strategy splits up the over-modulation zones into two different zones. The reference voltage is to be tracked by using the reference and holding angles in the above two zones, namely zone-I and zone-II, respectively. Here, the range of the linear control of output voltage is increased by 10%. Bolognani and Zigliotto (1997) proposed a digital continuous control for the SVPWM inverter, where a unique algorithm achieves the smooth transition from the start of over-modulation to six-step operation (Figure 7).

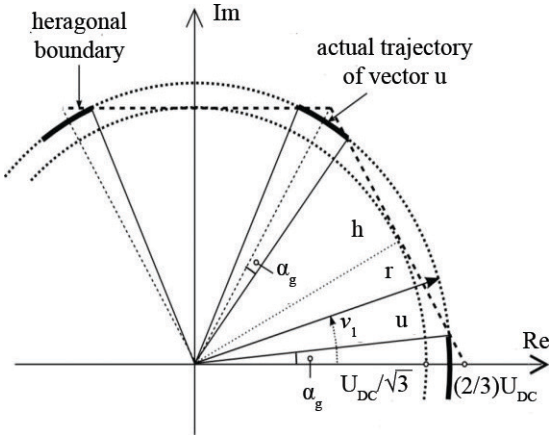


Fig. 7. The over-modulation strategy, as described in Bolognani and Zigliotto (1997).

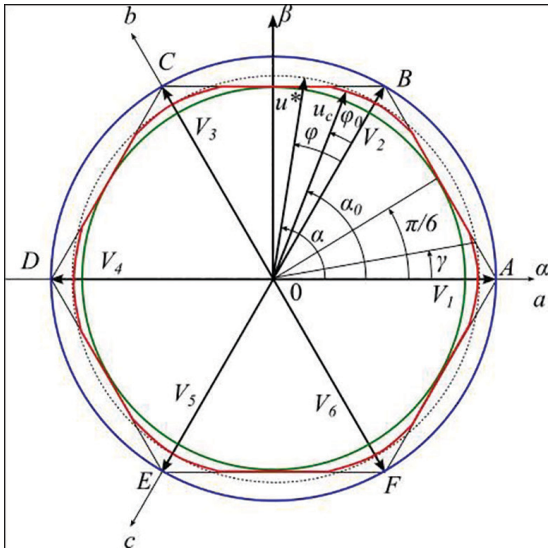


Fig. 8. Over-modulation using VCF (red line) (Ilioudis and Margaris, 2012).

Here, in a sector of the space-vector hexagon, the radius of the trajectory is increased until the trajectory intersects the hexagon boundary, and thereafter, it travels along the hexagon. The overall trajectory is determined with the involvement of the area matching principle, depending on the required amplitude modulation index. Thus, a simple implementation is possible, but the inverter loses its linear transfer characteristic and harmonics are generated accordingly. Attempts have been made to maximize the inverter gain, without generating lower-order harmonics. A look-up table-based SVPWM strategy to achieve a linear control of the inverter output voltage over the whole over-modulation range was presented in Lee and Lee (1998). Here, the amplitude modulation index is linked with the reference and holding angles. The reference angle is the angle of intersection of the compensated reference trajectory with the hexagon boundary. The holding angle controls the time interval for which the active switching state remains at the vertices of the space-vector hexagon, which uniquely controls the fundamental voltage. Here, reference angle and holding angle values are based on Fourier series expansion of the desired output voltage. In this algorithm, even-order harmonics and triple-n harmonics are eliminated in the output voltage. A unified algorithm, using a simple amplitude-phase correction technique, for regulating the voltage of an inverter in over-modulation region, has been introduced in Ilioudis and Margaris (2012). Here, a compensated voltage function is developed as shown in Figure 8, where u*/_α denotes the original reference voltage trajectory, and $u_c/\_\alpha_0$ is the compensated voltage trajectory, both with respect to the α axis. The corresponding angles with respect to the other sector-bounding active vector are φ and φ_0, respectively. Here, |uc| is equal to $V_{DC}/\sqrt{3}$ | g0 |, where g0 is called voltage

correcting function (VCF). The choice of |uc| determines fundamental as well as harmonic components of voltage. The VCF remains symmetrical in each sector with respect the angle π/6 and piecewise continuous over whole SVPWM area. This enables continuous transition from the linear modulation up to the six-step mode.

Different synchronised SVPWM strategies have been developed, which increase the DC-bus utilisation with reduced lower-order harmonics. Different control variables are chosen in different techniques, which are used in pre-modulation procedure. It is attempted to make the voltage control characteristics linear or piecewise linear and some of the techniques also result in lower peak current as compared to conventional space-vector strategy. Four space-vector-based synchronised PWM strategies, using pre-modulation technique, have been developed for low-switching-frequency inverters used in high-power drives (Narayanan et al., 2001). These are: (a) conventional space-vector strategy, (b) basic bus-clamping strategy, (c) boundary sampling strategy, and (d) asymmetric zero-changing strategy. Here, in every sub-cycle, the sample of the reference vector must first be corrected before being used for PWM calculations. In over-modulation zone-I, reference voltage vector is modified without any change in reference angle, whereas in over-modulation zone-II, the reference angle is modified using an angle correction factor, and reference voltage vector is changed therefrom. The voltage control characteristics are approximately linear or piecewise linear, which help in easy implementation and result in lower harmonic distortion. Another modified two-zone algorithm is introduced in Narayanan and Ranganathan (2002a, 2002b), which uses circular trajectory radius and angle correction factor as control variables in over-modulation zones I and II, respectively. Here a pre-modulation operation is done prior to PWM calculation (Figure 9). During pre-modulation, for maintaining the modulator gain constant, the inverse of the appropriate voltage control curve is used. The distortion becomes much lower in this algorithm, as compared to the one-zone algorithm, but remains higher than that in the two-zone algorithm, in zone-II. But However, this algorithm provides more simple voltage control characteristics, as compared with the two-zone algorithm. Two synchronised bus-clamping PWM strategies, named basic bus-clamping strategy-II and boundary sampling strategy-II, were proposed by Narayanan and Ranganathan (1998, 2002a, 2002b). These strategies are combined for producing the PWM waveforms with any odd pulse number, with the waveform symmetries preserved. The unclampable phase is switched an odd number of times within the sector and starting from the centre of the sector. On the other hand, the two clampable phases undergo an equal number of switching, either odd or even, within the sector. These two strategies result in lower harmonic distortion and lower peak current as compared to the conventional space-vector strategy, in the high speed ranges of high-power induction motor drives.

Generalised techniques involving multiphase system can be developed using SVPWM for increasing DC-bus utilisation and reducing lower-order harmonics, from which the three-phase system can be taken care of. Application of SVPWM in multiphase system in linear and over-modulation regions has been presented in Prie to et al. (2014). Each of the 2^n switching states of n-phase system develops a voltage vector, which is mapped into (n–1)/2 different orthogonal planes. An optimal solution has been proposed, where (n–1) adjacent active vectors are linearly combined and applied to form v_{ref} as shown in Figure 10. In this figure, v_{a1}, v_{a2}, … and v_{b1}, v_{b2}, … etc. are active vectors, which are combined with zero vectors to obtain the actual output vector. When reference voltage is within the over-modulation region, then in each sector at any position, the zero-vector duration is forced to zero. This reduces lower-order harmonics.

In some techniques, the pulse-dropping phenomenon disturbs the implementation of the algorithm, whereas in some other techniques the pulse-dropping method itself has been used to develop a process to maintain the required waveform quality. In Stumpf and Halász (2018), harmonic loss-optimised PWM control methods in the over-modulation region have been developed. Here, the lowest loss factor is proportional to the square of the RMS value of current harmonics, and the weighted Total Harmonic Distotion (THD) of the voltage is the square root of the loss factor. However, in this case, the matching process, between the output voltage fundamental component and the reference signal, is disturbed owing to the pulse-dropping phenomenon, which again pollutes the voltage

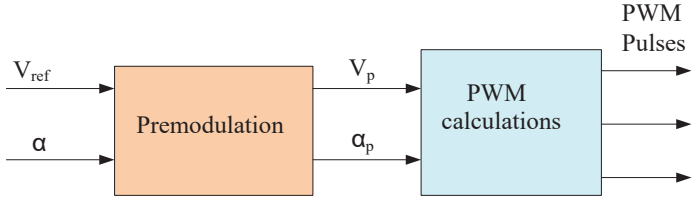


Fig. 9. Pre-modulation for over-modulation and linearity (Narayanan and Ranganathan, 2002a,2002b).

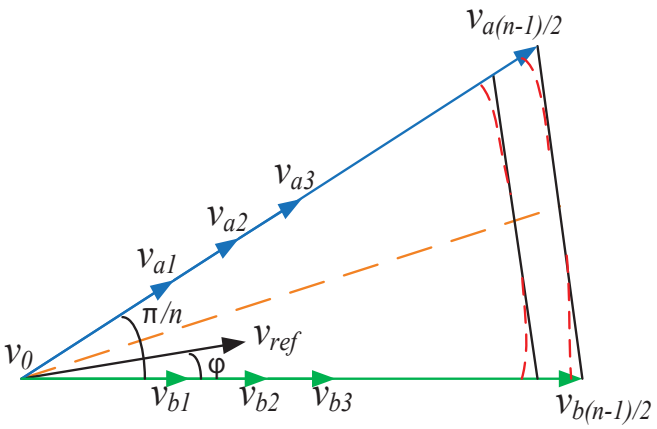


Fig. 10. Active voltage vector selection in α–β plane in SVPWM algorithms for *n*-phase drive (Prieto et al., 2014).

spectrum. Thus, reduction of the injected low-order voltage harmonic components is also one of the objectives of this work. A space-vector based discontinuous modulation technique has been proposed in Park and Youn (2003). It is designed in time domain and uses a pulse-dropping method. In the over-modulation region, it maintains the required waveform quality with a very wide modulation range. However, the hexagonal space-vector boundary puts a limit on the extent of the linear modulation range.

Several CBPWM techniques have been developed, where dynamic over-modulation characteristics are studied, which helps in developing new techniques. These techniques include phase-error regulation, generation of inverse gain function, adaptive third-harmonic injection etc. In Hava et al. (1998a, 1998b), waveform quality and voltage gain characteristics of CBPWM techniques in over-modulation region have been discussed. Here, the fundamental component of the reference modulation wave is multiplied with an inverse gain function to cancel the nonlinearity. Closed-form calculation of the inverse gain function is not very easy. Hence, a look-up table-based approach has been adopted in this work. These carrier frequency independent modulators require a wide modulation signal range, which reduces the resolution of the modulation waveform, degrading the performance. Besides, substantial subcarrier frequency harmonics remain in the inverter output voltage. The dynamic over-modulation characteristics of carrier-based current-regulated high-performance PWM VSI drives are detailed in Hava et al. (1999). Here, an algorithm with a phase-error regulation method having better performance is developed using direct digital PWM technique. Here, the time length of the two adjacent active inverter states can be determined using a complex volt-second balance equation. When the reference voltage vector tip lies outside the space-vector hexagon, the reference voltage vector is modified and at least one back-step calculation is carried out to avoid a negative time length. However, at a high speed of drive systems, the modulator voltage capability in the over-modulation zone is not sufficient, which may affect the steady-state and dynamic responses. In CBPWM, there is a degree of freedom in zero-sequence voltage selection and thus diverse PWM techniques can be developed (Badsi et al., 2016). Classical SVPWM technique delivers maximum modulation index, almost the same as third-harmonic injected PWM (THIPWM). In the D-PWM$_{Max}$ technique, the zero-sequence voltage is added in discontinuous PWM (DPWM) mode using the maximum magnitude test of three sinusoidal waveforms, whereas in the D-PWM$_{Min}$ technique, the same is added using the minimum magnitude test. In both these cases, increase in modulation index in linear modulation region has been observed. In Albatran et al. (2021), two adaptive optimal third-harmonic injection techniques (AOTHI-PWM) are presented for maximising the DC-bus utilisation and minimising voltage THD in a grid-connected inverter. From here, one generalised AOTHI-PWM is framed using polynomial and rational regression models. However, in this scheme, the DC bus becomes distorted, as it is not possible to completely eliminate the injected grid harmonics. This can affect the DC-bus controller, which then generates an oscillated current reference, resulting in the grid current distortion.

From the above discussion, it can be observed that improving the DC-bus utilisation by traversing into the over-modulation zones generally increases lower-order harmonic content and output distortion. The control characteristics become nonlinear and sometimes, owing to pulse dropping, switching losses are reduced. Hence, some optimisation-based strategy may be sought for, which will give optimal improvement on most of these fronts.

2.2. Switching-loss reduction in linear and over-modulation zones of PWM inverter

In PWM inverters, the dominant harmonics come as side-bands of switching frequency and/or its multiples. Hence, the switching frequency is usually chosen in such a way that it is much higher than the modulating frequency. Thus, filtering the dominant harmonics becomes easy, but switching loss associated with this process is increased. Several researches have been carried out and are also going on for proposing PWM strategies, which can reduce switching loss, while achieving the same level of performance as normal PWM inverters.

To reduce the switching losses in an inverter, attempts have been made to develop a hybrid modulation technique, where the switches of any of the legs are made continuously on or off for a certain duration, whereas the switches of the other legs are turned on and off at switching frequency. This is equally applicable for all the legs of the inverter. Different algorithms have been developed for implementing the above concept. A technique to reduce switching losses in three-phase PWM inverters was introduced in Dunford et al. (1994). In this technique, at any point on the cycle, the minimum phase voltage is to be identified and all phase voltages are reduced by that amount. The minimum phase pulse width is always set to zero and the relevant inverter leg is set permanently low (equal to negative DC-bus voltage) for part of the cycle. The significance of this technique is that, only two legs rather than three are switching at any instant, resulting in a switching-loss reduction of one-third. A hybrid PWM technique has been proposed in Lai and Ngo (1995), which requires PWM of only two of the four switches in a full-bridge inverter at high frequency (a few kilo-hertz), while the other two switches are operated in square wave mode at output frequency. Thus, in the other two switches, the switching losses are reduced significantly. However, for reducing the current or voltage stresses on the main switches, auxiliary switches and diodes would be required that have ratings higher than that of main switches. It has also restriction on load types and limitation on duty ratio. This theory has been extended to three-phase inverter in Li et al. (2008). Here, two of the six switches are not operated at the switching frequency, which results in reduced switching loss. In regions 0^{o}–60^{o}, 120^{o}–180^{o}, and 240^{o}–300^{o}, the lower switch for the phase with minimum voltage is always kept turned on, and the corresponding upper switch for this phase is always kept turned off. The reverse is the situation for 60^{o}–120^{o}, 180^{o}–240^{o}, and 300^{o}–360^{o}, which is determined by the phase of maximum voltage. Cavalcanti et al. (2002) deals with two PWM schemes, where the switching sequences can easily be implemented for three-phase quasi-resonant DC link (QRDCL) inverter by using the hybrid modulation concept and without involving look-up tables. Here, apportioning factor is varied for implementing the hybrid modulation. This strategy dealt with PWM schemes, which synchronise clamped voltage segments using the current peak in corresponding phases of a three-phase QRDCL inverter. In all ranges of phase-angle variation, the clamping interval distribution in accordance with the phase angle between the output current and voltage helps in loss minimisation. Here, switching frequency is reduced owing to absence of switching during the peak of the output currents.

In some of the techniques, the switching frequency is varied, instead of being maintained constant. This may be through uniform distribution of the switching frequency, or pre-computed switching-frequency-variation factors, or by mathematical optimisation procedure etc. In most of the cases, there is a limit in the range of its variation, which may be different for different techniques depending upon some of the aspects of the concerned technique. For reducing conducted EMI and for eliminating the EMI spikes, a novel PWM technique, called uniform distribution PWM, is developed in Chen et al. (2020). Its design depends on the uniform distribution of the switching frequency and achievement of reduced switching loss. The number of sampling points used to implement this strategy is based on a switching-frequency distribution function. Here, the switching-frequency variation range is fixed for any modulation index. However, the suppression of EMI effect depends on waveform characteristics. For reducing the switching losses and maintaining the peak–peak current ripple within a preset limit, Bhattacharya et al. (2017) presented a switching-frequency variation scheme. Instead of depending on optimisation or prediction methods, the proposed technique uses pre-computed switching-frequency variation factors. Here, the operating carrier ratio and modulation index are the basic factors to be considered for the switching-frequency variation. The switching-frequency coefficients are calculated and stored in a look-up table. The base switching frequency is then multiplied by these coefficients to obtain the inverter operating switching frequency. The coefficient adjustment factor puts the limit to the switching-frequency excursion at a lower current ripple. Thus, the system response is not affected by lower switching frequency. However, the low-order harmonics are increased as compared to an identical PWM method with constant switching-frequency carrier. In grid-connected photovoltaic (PV) application, Mao et al. (2009) developed a variable switching-frequency-based technique for minimising the switching loss, where a given THD requirement is also maintained. This strategy has two sub-parts: the constant ripple (hysteresis control) scheme and the optimal scheme. The strategy is based on current-ripple analysis in time domain and the calculus of

variations. Apart from a significant reduction in switching loss, other benefits such as a spread spectrum of the current harmonics and reduced peak switching loss are also achieved. In Oñederra et al. (2017), the variation of the switching frequency is done with the output current-ripple RMS value over the fundamental period, resulting in a lower number of commutations. The presented technique is executed by mathematical optimisation and is applied to a real system involving different loads and modulation indexes. This method reduces high-power side losses and driving losses without increasing load losses. However, such a variable frequency strategy cannot be accurately implemented without the aid of a suitable model of the DC-link voltage ripple.

Different DPWM techniques have been developed, where the phase segments are clamped to the DC rails. This makes the switches continuously on or off for a certain duration and reduces the switching loss of the inverter. Here, the modulation signals are derived through different techniques e.g. using an existence function or already given duty factors and through common-mode signal injection etc. A generalised DPWM (GDPWM) can be derived, which helps in forming different types of DPWM techniques therefrom. In DPWM scheme, phase segments become clamped, either to the positive or negative rails, using modulator with discontinuous zero-sequence signal (Ojo and Kshirsagar, 2003).This phase segment clamping reduces the switching loss. The expressions for the discontinuous modulation signals are derived by averaging their existence functions for every space-vector sector. The reference voltage is realised from the average i.e. the first term of the Fourier series expansion of the existence function, which is equal to the sum of the turn-on times of each device in its normalised form. Various GDPWM waveforms can be generated using the generalised expression for modulation signals taking modulation angle as a control parameter of GDPWM. Depending upon zero-sequence signal addition at different values of modulator phase angle, different DPWMs such as DPWM1, DPWM2, and DPWM0 can be generated as modulation signals. For DPWM1, the centre of the DC rail clamped segment is aligned with peak of the cosine modulating wave; in DPWM2 there is a 30° phase difference between them. In both cases, the highest current is conducted through DC rail clamped switch, resulting in minimum switching losses. Merely a single DPWM choice cannot provide improved performance in all aspects. A high-performance GDPWM method and an algorithm have been presented in Hava et al. (1998a, 1998b). The modulation waves for different modulation phase angles are shown in Figure 11. Combining GDPWM with SVPWM, using harmonic distortion factor (HDF) curves, maximises the drive performance in the whole modulation range. With DPWM methods, the switching losses are significantly influenced.

In some techniques, the switches are clamped to DC bus for a certain duration. This reduces the number of switching resulting in DPWM and reduced switching loss. This may use pulse-dropping method, adjustable DPWM, injection of common-mode signal etc. It has always been attempted to achieve a seamless transfer from continuous to DPWM and vice versa. A new SVPWM technique, based on discontinuous pulse-dropping method in time domain,

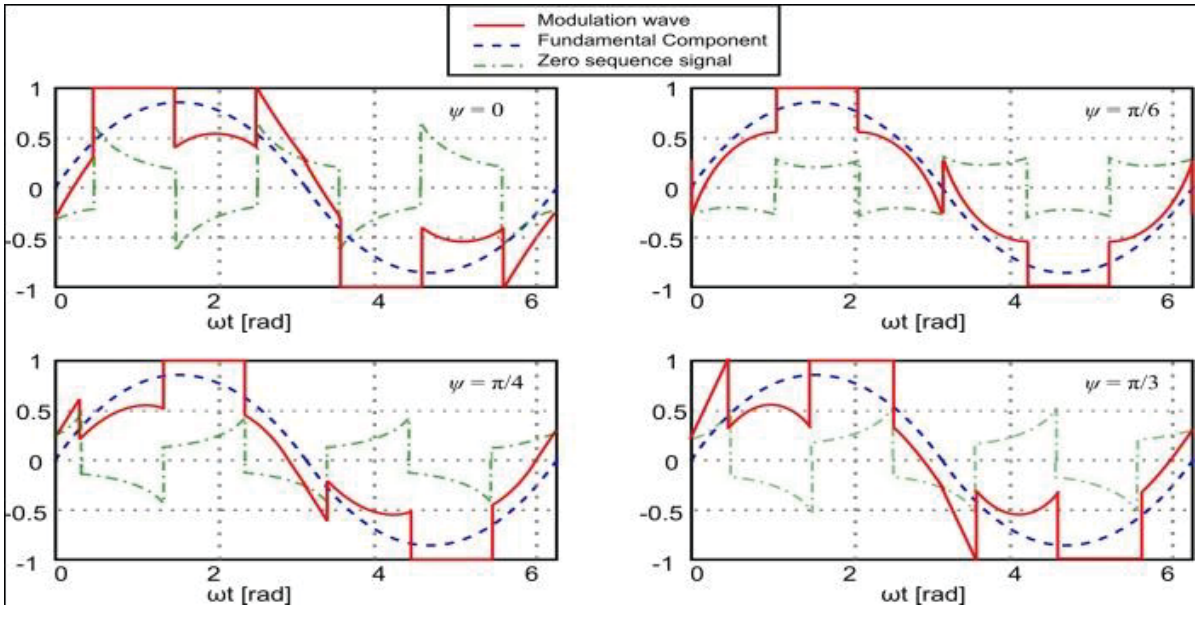


Fig. 11. Modulation waves ('–'), fundamental component ('– –'), and their zero-sequence signal ('–·') for Mi = 0.7 and four different modulator phase-angle values (Hava et al., 1998a,1998b).

has been proposed in Park and Youn (2003). This reduces the number of switching in the inverter, which results in switching-loss reduction. Here, the reference voltage vector is calculated from given duty factors. However, the use of the pulse dropping in the proposed control method reduces switching loss at the cost of increasing lower-order harmonics. Hence, the use of this method is limited to only the over-modulation region of operation. An adjustable DPWM technique has been proposed in Lee et al. (2015). This is shown in Figures 12 and 13. Here, non-switching period is controlled from 0° to 120° of fundamental period by a weighting factor k, which is calculated by modulation index m_a and discontinuous angle θ_D, measured from the positive peak of a modulating waveform. In this case, θ_D is linearly proportional to m_a. If θ_D is set as 0° and 30°, adjustable DPWM becomes similar to symmetrical SVPWM, and 60° DPWM, respectively. Thus, if θ_D is gradually increased from 0° to 30°, the seamless transfer from SVPWM to 60° DPWM is wholly possible. This technique offers a trade-off between THD and switching loss through seamless transfer from CPWM to DPWM. An adaptive DPWM method has been proposed to adjust the injected common-mode signal with the modulation index (Liu et al., 2017). This is represented in Figures 14 and 15. With low modulation index, a large CM wave is injected. The reverse is the situation for high modulation index. In adaptive DPWM, between positive and negative clamping interval, a varying coefficient is set to adjust the mode wave transition slope. Here, for the low modulation index case, slow transition is implemented, whereas for the high modulation index case, fast transition is implemented. Owing to the injection of this CMV, the resultant modulating waveform gets clamped, which results in reduced number of switching and corresponding loss.

In this area there are several recent publications, which report new techniques capable of reducing the switching loss without affecting other performance parameters or with some additional features involved. For reducing the

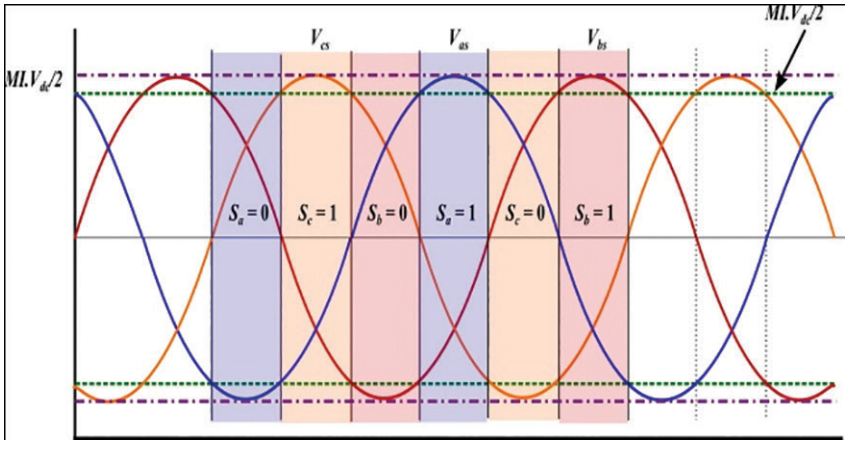


Fig. 12. Switching patterns and phase voltage references for 60° DPWM (Lee et al., 2015).

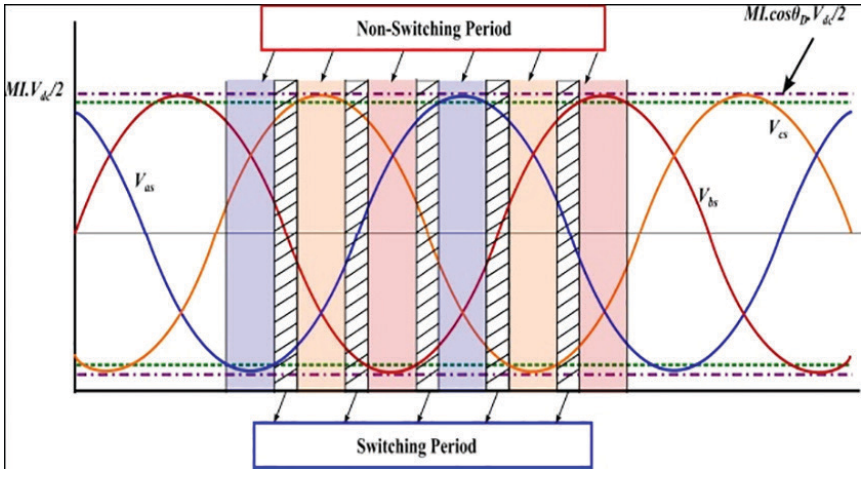


Fig. 13. Switching patterns and phase voltage references of proposed adjustable DPWM (Lee et al., 2015).

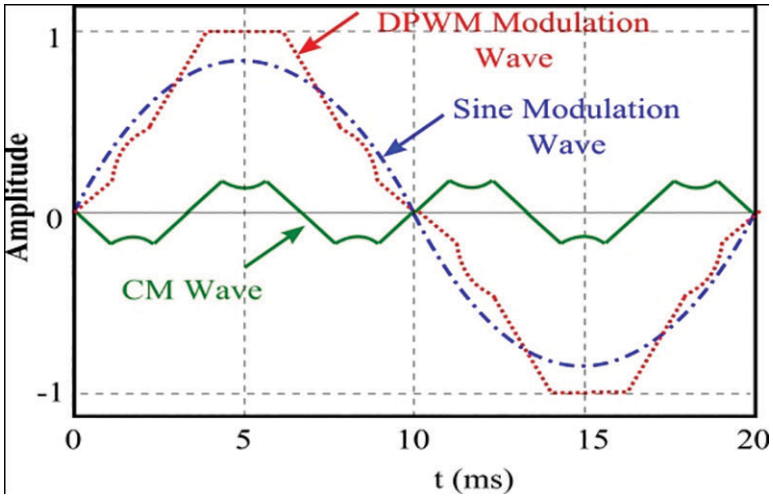


Fig. 14. Modulation waves in adaptive DPWM for m_a = 0.88 (Liu et al., 2017).

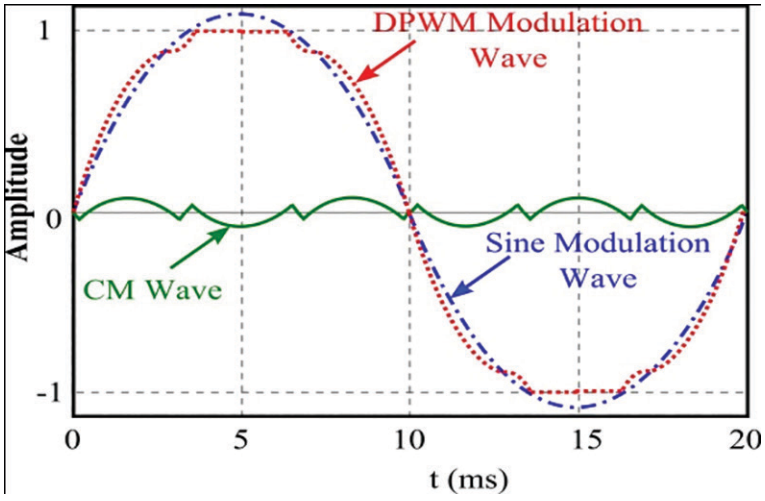


Fig. 15. Modulation waves in adaptive DPWM for m_a = 1.1 (Liu et al., 2017).

switching losses and increasing the frequency of the PWM sideband voltage, Huang et al. (2020) presented a modified single-edge space-vector PWM method (MS-SVPWM). The MS-SVPWM is developed from the centre-aligned SVPWM by exchange of the active vectors for increasing the carrier PWM harmonic frequency to double at the expense of increasing the average switching frequency by 33%. This also adjusts the zero vectors of saw-tooth carrier SVPWM. An online technique is proposed in Xu and Lu (2021) for dynamically computing and selecting the lower current-ripple sequence throughout the vector space. Here, an online optimal modulation scheme is developed using the intuitive perspective of current-ripple minimisation per switching cycle, maintaining the switching frequency as the same. Here, extra switching during the sequence swapping is avoided, which results in even less switching losses. The presented control technique has a fault-tolerant feature and can also reduce the general switch losses with reduced conduction current.

This section has discussed several bus-clamping based PWM strategies and other such hybrid PWM techniques, based on which switching losses may be reduced in a PWM inverter. While such techniques may be quite successful in terms of achieving reduced switching loss, it is often observed that adoption of such techniques may lead to other performance-based shortcomings in PWM inverters, such as introduction of lower-order harmonics, reduced control bandwidth etc. From the above discussion, it has been found that optimal operation of GDPWM or hybrid PWM technique based inverter in a closed-loop strategy, considering the fluctuations of input DC-bus voltage, output load, and power-factor while maintaining low switching loss and THD, may be investigated further.

2.3. CMV aspects and PWM strategies reducing it

In a three-phase two-level inverter, the voltage between the mid-point of the DC bus and the neutral point of the load is defined as its CMV. Generally, the triplen harmonic components are available in the CMV (Bose, 2002). In electrical drives, CMV variation, resulting from the switching of the power devices, is one of the important problems under discussion. It causes unwanted phenomena such as high levels of EMI, degradation of ball bearings in electrical machine etc. These problems develop as an outcome of the flow of parasitic capacitive currents, generally known as common-mode currents (CMCs), which arise as an effect of CMV variation. Reduction of CMCs is essential for increasing electromagnetic compatibility and the reliability of electric drives. SVPWM has almost the same behaviour regarding the CMV variation as sine-triangle PWM.

Numerical simulation has been done in the MATLAB Simulink digital platform to show the CMV profile in conventional SPWM and SVPWM technique based three-phase two-level inverter in different operating regions. The operating regions as well as the simulation parameters have already been mentioned in Section 2.1. The inverter CMV profile for SPWM technique in linear region and SVPWM technique in different operating regions without considering the dead-time effect are shown in Figures 16–19.

Several works have been reported over the past few decades, which present new PWM techniques or modify the already existing techniques for reducing the CMV of the inverter. In some cases, simultaneous application of zero-voltage vectors (ZVVs) and specific active voltage vectors is avoided, whereas in some techniques, the neutral voltages of the active and zero vectors are averaged. A random inverter control technique, as presented in Lai (1999), reduces the CMV and also the dominant harmonic cluster of PWM output voltage. The number of commutations for inverter control is not made constant in a carrier period for reducing the dominant cluster in the harmonic spectrum of voltage/current. The random switching scheme does not create any change in the sampling

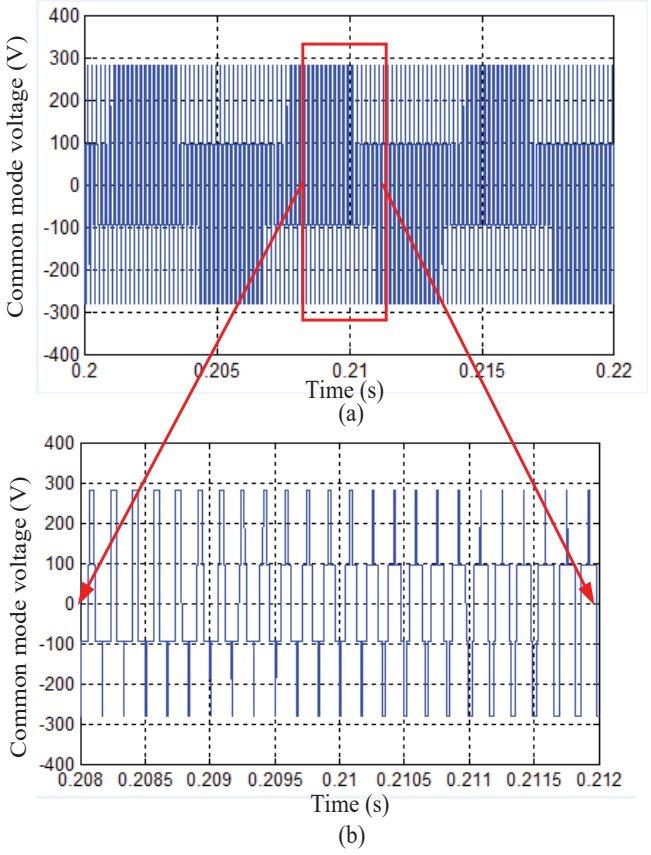


Fig. 16. Inverter common mode voltage in linear region of SPWM without dead time (a) showing its low-frequency profile (b) in expanded scale showing its high-frequency profile.

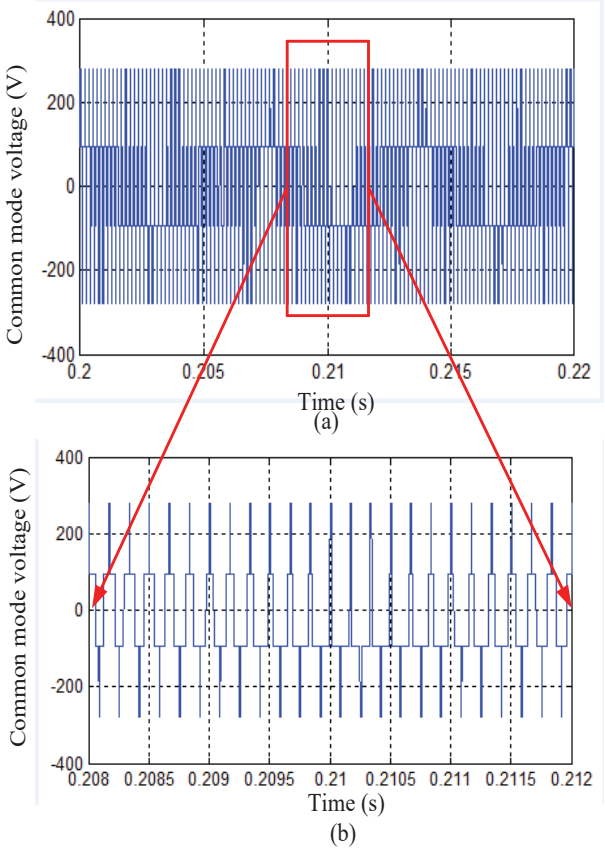


Fig. 17. Inverter common mode voltage in linear region of SVPWM without dead time (a) showing its low-frequency profile (b) in expanded scale showing its high-frequency profile.

technique. Thus, it can be easily added into existing the inverter control system with only minor modifications in the switching patterns. The random switching technique reduces the CMV to around 50% in comparison with that for conventional random SVM (RSVM) technique. It therefore reduces the cost of using EMI filter. Lee and Sul (2001) proposed a new SVPWM strategy with the synchronisation of the switching sequence, which can reduce the inverter CMV within one-third of DC-bus voltage. The inverter active voltage vector is shifted in a control period and an inverter switching point is synchronised with a converter switching point. This avoids the simultaneous application of the combination of ZVV and specific active voltage vector. It eliminates the CMV pulse of magnitude $2V_{DC}/3$, and reduces the number of pulse of common mode to two in one control period. The proposed technique does not require extra hardware and can be implemented easily in software and without any inverter control performance degradation. However, this technique, without zero states, uses parts of the voltage vectors and loses the degree of freedom of the redundant vectors. This results in larger current ripples, especially in case of low voltage. Also, it cannot be applied to current-source converters, because of different CMV generation mechanisms. Averaging of the two neutral voltages of the two active and two null vectors of the space vector is done to determine the analytical expression for the generalised neutral voltage waveform (Ojo, 2004). Using this method, the waveform quality can be improved, CMV of inverter fed motor drives can be considerably reduced, and the linear modulation range can be extended.

The conventional SVPWM is often modified to reduce the CMV of the inverter. This may be achieved by using only-odd or only-even vectors or introducing virtual space vectors derived from the original stationary vectors. The basic aim is to modify the switching pattern so as to reduce the level of variation of the CMV per switching cycle. Modified space-vector modulation (MSVM) is an excellent way for reducing CMC generation (Cacciato et al., 2009) and is represented in Figure 20. Here CMV is maintained constant to $V_{DC}/3$ or $2V_{DC}/3$ in the whole sector. There is no variation of the CMV while switching from any even to another even state or from any odd state to

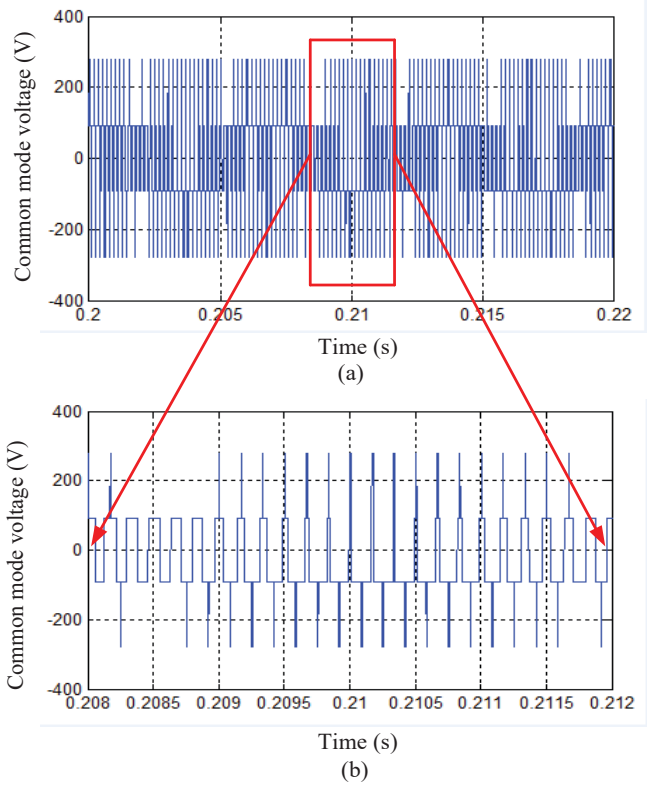


Fig. 18. Inverter common mode voltage in over-modulation-I region of SVPWM without dead time (a) showing its low-frequency profile (b) in expanded scale showing its high-frequency profile.

another odd state. In such switching technique, the average reference voltage is obtained by switching between the odd inverter states i.e. VI, V3, and V5 for the only-odd modulation and between the even states V2, V4, and V6 for the only-even modulation. Odd-zero PWM (OZPWM) has been proposed in Noroozi et al. (2017), which is a novel modulation technique based on reduced common mode (RCM) method. In this technique, two adjacent odd vectors and zero vector (000) are used. Here, at the beginning and end of each switching cycle, the zero vector is applied. In the presented method, reduction in the number of fluctuations of the CMV waveform per switching cycle occurs, resulting in a decrease in the amount of high-frequency harmonics of CMV. With the application of active and zero vectors in the proposed strategy, the total harmonic distortion becomes less as compared to most of the other reduced RCM methods. A virtual space-vector modulation (VSVM) technique having zero average CMV was proposed to reduce both the magnitude and triple-n component in CMV (Tian et al., 2016). Here, three variants of this technique, namely VSVM1, VSVM2, and VSVM3, are developed using nine virtual space vectors derived from original stationary vectors. The choice of zero magnitude virtual vectors creates the difference among VSVM1, VSVM2, and VSVM3 [Figures 21 and 22]. In VSVM1, V36 is selected, whereas in VSVM2, V25 is selected, and for VSVM3, V36 is used for $\pi/6 \leq \theta < \pi/3$ and V25 is used for $0 \leq \theta < \pi/6$. Here, the overall gain of the inverter gets reduced. A finite state model predictive control (FS-MPC) technique having constant switching frequency and low sampling frequency applies a discrete space-vector modulation (DSVM) strategy, as presented in Vazquez et al. (2009), and shown in Figures 23 and 24. In DSVM technique, a finite number of virtual vectors are synthesised by a linear combination of the converter discrete real states and can be placed anywhere in the converter control region. Here, the real state vectors of the converter are used together with new virtual state vectors. However, MPC-DSVM involves either a look-up table or an external modulator, which involves a more complex control hardware.

Instead of using conventional active-zero-state PWM (AZSPWM), new AZSPWM techniques have been introduced, either through software implementation or through change in topology. In many of the reduced CMV methods, the zero vectors are not applied directly but generated using active vectors. An algorithm is developed for generating inverter output voltage with reduced common-mode content in Rangarajan et al. (2010). This technique

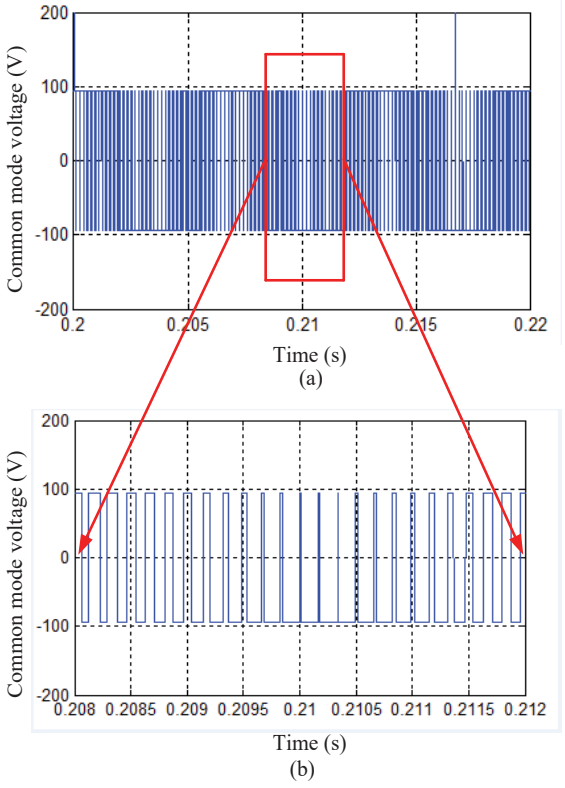


Fig. 19. Inverter common mode voltage in over-modulation-II region of SVPWM without dead time (a) showing its low-frequency profile (b) in expanded scale showing its high-frequency profile.

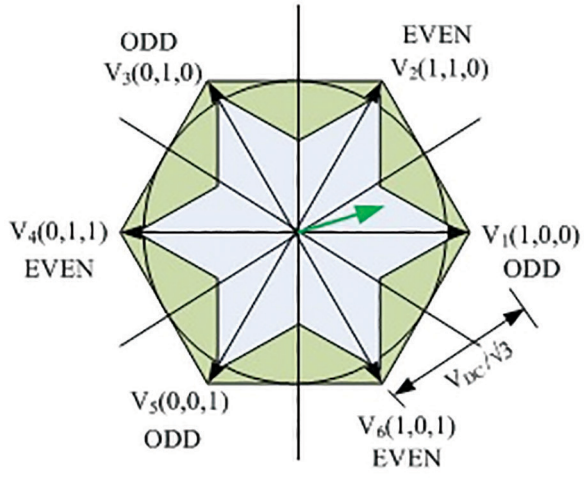
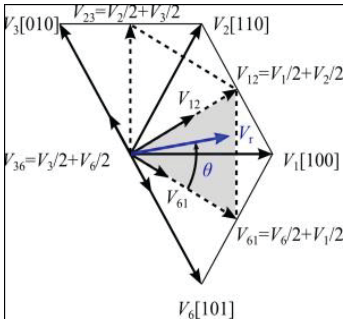
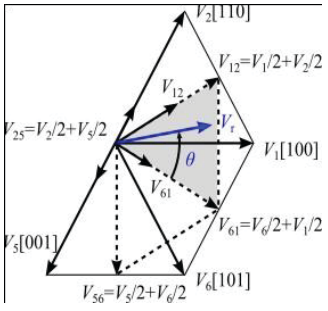


Fig. 20. Linear zone limit by exploiting the proposed approach (Cacciato et al., 2009).

also includes compensation for reflected-wave motor overvoltage stress and dead time. While conventional three-phase PWM techniques combine active vector states and zero vector states for producing the required output voltage, the reduced CMV PWM techniques involve only active vector states for reducing CMV significantly. Simultaneous switching of two phases is prevented by implementing different switching logic in odd and even sectors in space-vector hexagon. This avoids the spikes in the CMV at sector transitions. In transient conditions, the reference vector can jump between arbitrary sectors. Then, the appropriate sequence type is chosen for avoiding

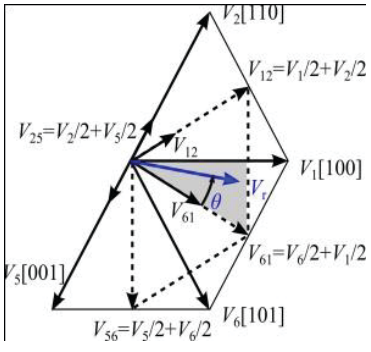


(a)

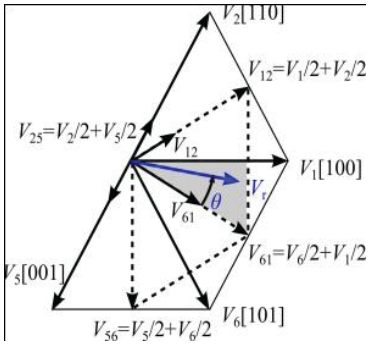


(b)

Fig. 21. Illustrating virtual space-vector concept in the proposed (a) VSVM1 and (b) VSVM2 (Tian et al., 2016).



(a)



(b)

Fig. 22. Illustrating virtual space-vector concept in the proposed VSVM3: (a) when $\pi/6 \leq \theta < \pi/3$, (b) when $0 \leq \theta < \pi/6$ (Tian et al., 2016).

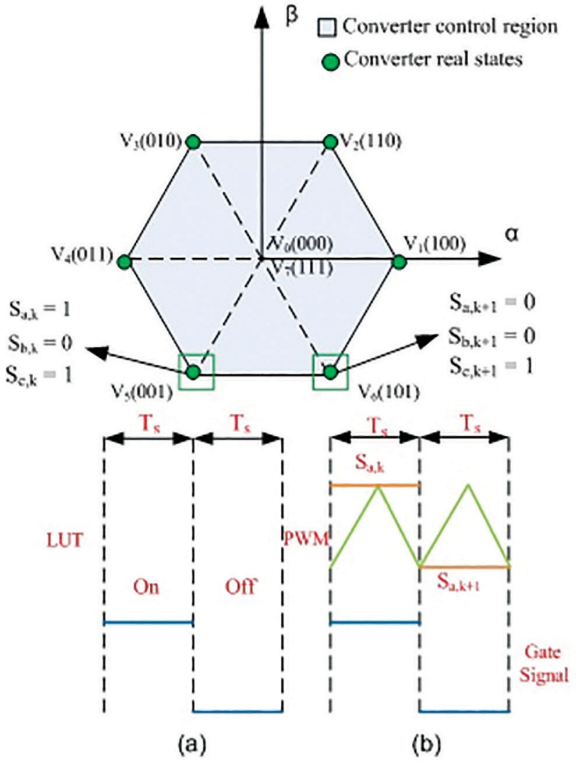


Fig. 23. Generation of switch firing pulses in FS-MPC: (a) using look-up table, (b) using external PWM modulator (Vazquez et al., 2009).

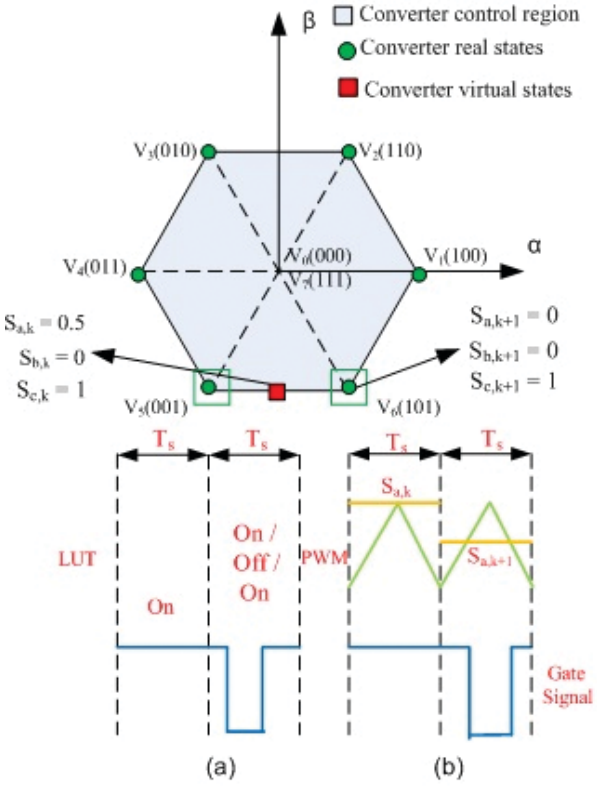


Fig. 24. Generation of switch firing pulses with MPC-DSVM: (a) using look-up table, (b) using external PWM modulator (Vazquez et al., 2009).

CMV spikes during the transition. A high-performance PWM algorithm has been developed combining the near-state PWM (NSPWM) technique having better performance characteristics at high modulation index and modified active-zero-state PWM (MAZSPWM), suitable for low modulation index range of operation (Hava and Ün, 2011). NSPWM involves the three near active voltage vectors for programming the desired output voltage. MAZSPWM involves two adjacent voltage vectors with two opposing active voltage vectors, but reorganises the duty cycles of the voltage vectors to provide sufficiently large zero-voltage time intervals between pulse reversals. This avoids over-voltages during pulse reversals. The algorithm has satisfactory performance over the entire operating range of inverter, and seamless transition from NSPWM to MAZSPWM and vice versa is achievable. SPWM with interleaved carriers (Kimball and Zawodniok, 2011) reduces the zero vectors, thus decreasing the CMV RMS value, but allows CMV peaks of half of the DC-link voltage. The carrier waves are displaced by one-third of a switching period from each other. Zero vectors can be totally eliminated by involving only active vectors in phase opposition and with equal duty cycles. No additional computation time is needed during operation. Fourier analysis shows that the CMV is significantly reduced by interleaving the carriers in conventional uniform PWM. The improvement depends on the sampling method and modulating function. At full modulation the CMV is reduced to around 36%, whereas it is reduced to around 67% during idling with zero modulation. However, at the switching frequency, there is an increase in current ripple. AZSPWM, as mentioned in Wu et al. (2016), uses two adjacent voltage vectors and two opposing active vectors having equal duty cycle for generating equivalent ZVVs. In current-ripple loss-optimised common-mode voltage reduction PWM (CRLO-CMVRPWM), the mean-square values of three-phase current ripples are minimised for optimisation of the output waveform characteristics. This is done by finding the optimised solutions of the volt-sec balance equations with the designed switching sequences. Furthermore, using CRLO-CMVRPWM, more than 23% switching losses can be reduced as compared to AZSPWM, in addition to obtaining better output waveform characteristics. To overcome the adverse effect of CMV, Zhang and Bazzi (2022) presented a new integrated active-zero-state switch (IAZS) topology, as shown in Figure 25. In IAZS, a new zero-state voltage

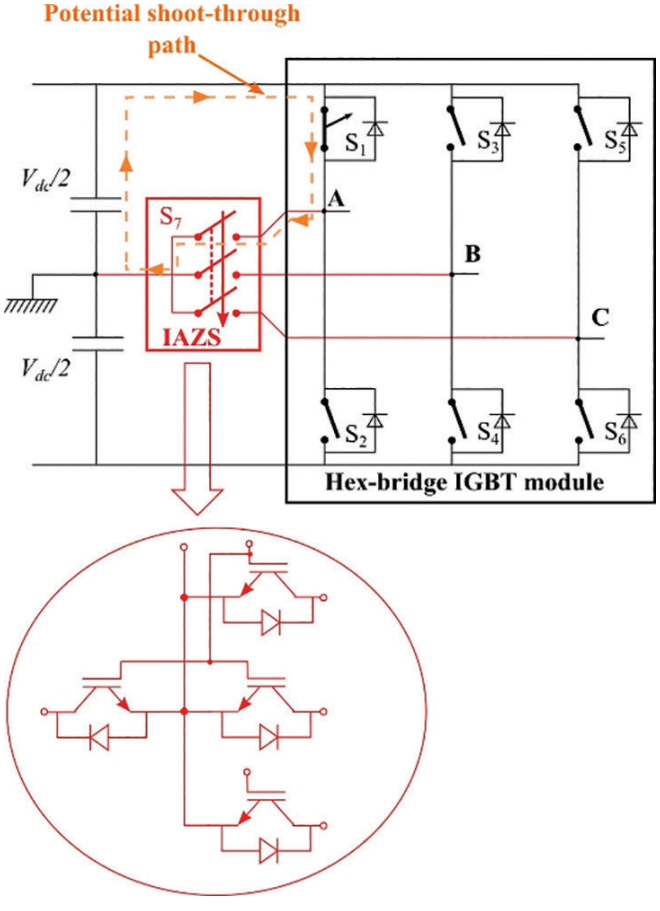


Fig. 25. IAZS based VSI topology (Zhang and Bazzi, 2022).

vector V8 (1xxx) is created, which results in zero CMV. Here, 'x' represents the state where both the upper and lower switches are inactive in one phase leg of the inverter. This V8 vector is used in place of the voltage vectors V0 (0000) and V7 (0111) for synthesising the output voltage V_{ref}. For facilitating the use of IAZS, minor adjustment to the standard SVPWM is required with the proposed topology. The important advantages of IAZS include its function as a 'plug and play' component without adding any complexity to the whole system and without impacting current THD.

A large number of research works have been undertaken where the change in topology has been executed or external circuits have been added for reducing the CMV. Some of the works change the basic structure of the inverter set-up. A few of the works involve external circuit for CMV reduction e.g. active common-noise canceller circuit (ACC) or a hybrid output EMI filter etc. However, this may increase the cost or complexity of the system. Duong et al. (2021) developed a three-phase impedance source inverter to reduce the common-mode voltage. An attempt to reduce CMV by using topological variation has been reported in Morris et al. (2017**)**, where the conventional inverter topology is modified by adding two switches in series in the DC lines. The principle is to open these extra switches disconnecting the DC source from the inverter, whenever the null-states are applied to the output, thereby reducing the CMV by a large extent. Owing to the presence of many parasitic elements in the system, it is not always practical to achieve 0 V during the floated zero states. The antiparallel zener diodes can be placed in parallel to the extra switch, to ensure a consistent CMV waveform having less variation. The presented topology has reduced CM voltage without adding complexity and can be applied with conventional control and PWM

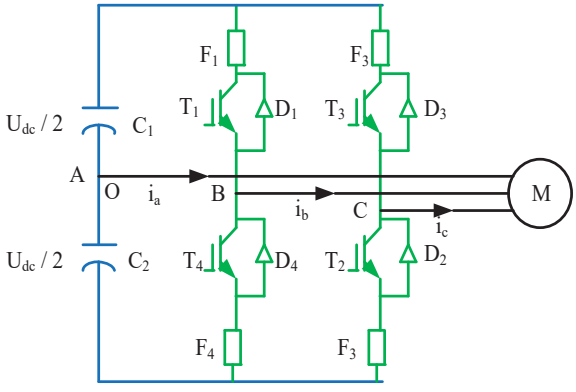


Fig. 26. Topology of a FSTPI-fed induction motor drive system (Li et al., 2017).

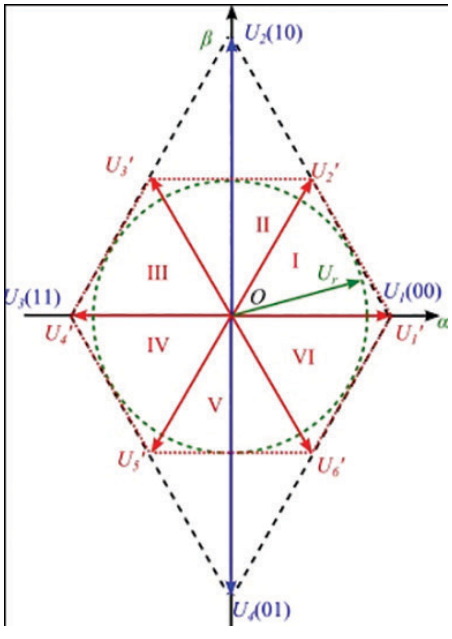


Fig. 27. Basic voltage vector distribution of FSTPI (Li et al., 2017).

schemes. The four-switch three-phase inverter (FSTPI) as shown in Figures 26 and 27 may be used in fault-tolerant control for solving the open or short-circuit fault in six-switch inverter (SSTPI) (Li et al., 2017). The FSTPI, based on virtual voltage vector, can generate only four active vectors in the α–β plane together with maintaining the zero vectors in an absent condition, which results in reduced CMV. Here, two active vectors U_1 and U_3 have an equal magnitude and one that is different from the U_2 and U_4 magnitude. Six virtual space vectors are developed using the four active vectors in FSTPI having different weighting coefficients. Compared to the traditional strategy, in the presented technique, the reference voltage vector is synthesised by using six newly developed voltage vectors U_1' to U_6', which avoids the calculation of the holding angle and the reference angle. Duong et al. (2021) utilized three-phase impedance-source inverter for reducing the common mode voltage. Ogasawara et al. (1998) presented an ACC. It consists mainly of a common-mode transformer and an emitter follower using complementary transistors for achieving active cancellation of CMV. In ACC, a compensating voltage is superimposed on the inverter output. This is with the same amplitude but of opposite polarity to the CMV produced by the PWM inverter. This results in complete cancellation of the CMV applied to a load. Moreover, the ACC can suppress motor shaft voltage and can prevent an electric shock on a motor frame in non-grounded form. Pairodamonchai et al. (2009) presented a hybrid output EMI filter for CMV reduction in PWM inverters. It consists of a single-leg four-level active filter connected in series with a small passive LC filter, which suppresses the CMV in the high-frequency range, and a series capacitor for blocking low-frequency components of the CMV. The PWM voltages at the inverter's output are detected through opto-isolators and are transmitted to the logic gate circuit for reconstructing the required CMV. The compensating voltage is fed to the three-phase line through a common-mode coupling transformer. The passive LC is used to enhance the filtering characteristics. However, the additional hardware results in a significant increase in the volume of the system or much more complex control techniques.

This section has addressed the issue of CMV and its problems. It has cited several studies in the literature that aim to solve such problems. However, it is observed that different techniques for reduction of CMV come with different problems, such as increased switching loss, increased complexity in control algorithm, reduction of overall inverter gain etc. A possible research direction in this field may be to formulate a CMV reduction technique without affecting other performance parameters.

2.4. Distortion of output voltage owing to dead-time effect and its compensation

Every solid-state switch takes a finite time to turn on and off. Thus, to avoid shoot-through fault in one leg of a two-level inverter, a finite time delay between the instants of turning-off of one switch and turning-on of the other switch of the same inverter leg is required. This time delay is called 'dead time' or 'blanking time', which introduces

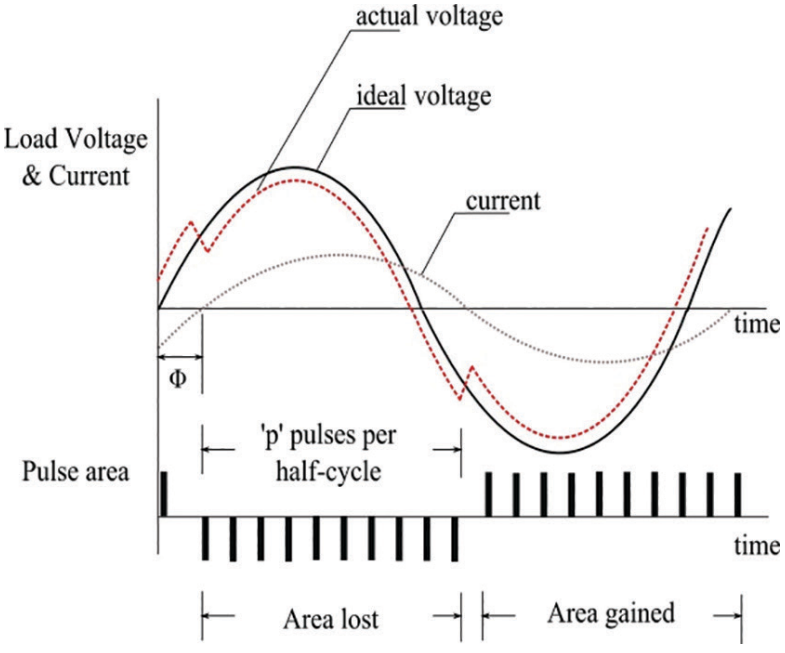


Fig. 28. Effect of dead- time distortion in output voltage (top) and pulse area lost and gained in each half cycle (bottom) (Dalapati, 2013).

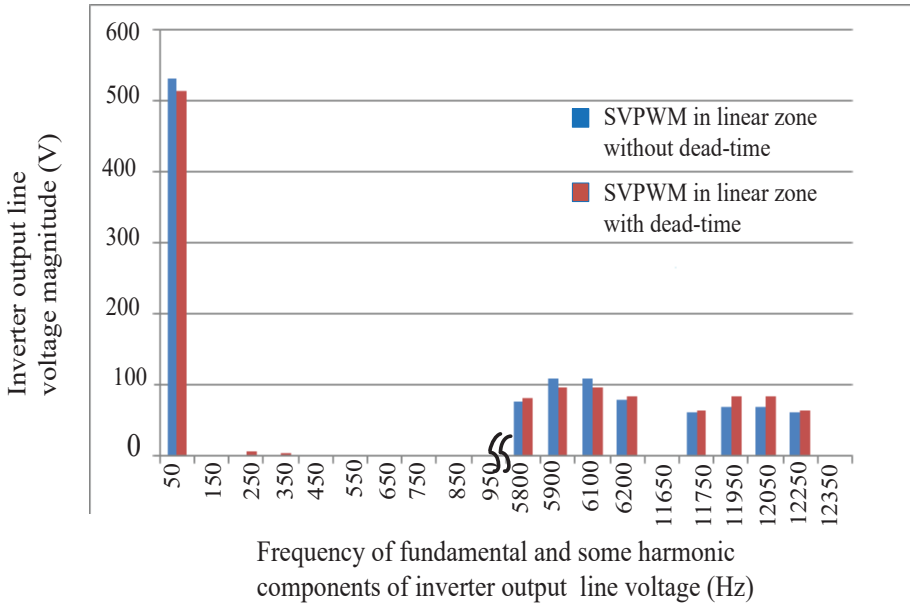


Fig. 29. Plot of the magnitude of the inverter output voltage (V) with frequency (Hz) in SVPWM technique in linear operating region with and without dead time.

distortion in the inverter output voltage waveform, as shown in Figure 28 (Dalapati, 2013; Mohan et al., 2009). As a result of this, lower-order harmonics are generated in output voltage and current waveforms. Owing to the pulse loss or gain in every switching cycle due to presence of dead time of the inverter, there is a loss in area of pole voltage pulses. This loss in pole voltage pulses, when averaged over a fundamental cycle of output voltage, clearly indicates a voltage drop, resulting in a reduction in output voltage. This voltage drop depends on switching frequency, deadtime, and DC-bus voltage.

Numerical simulation has been done in the MATLAB Simulink digital platform to show the effect of dead time on output voltage in conventional SPWM and SVPWM technique based three-phase two-level inverter in different operating regions. The operating regions as well as the simulation parameters have already been mentioned in Section 2.1. The effects of dead time on inverter output voltage for SPWM technique in linear region and SVPWM technique in linear operating region have been shown in Figures 5 and 29, respectively. Some of these research works involving analysis and mitigation of this distortion are discussed in the following paragraphs.

Several studies have been undertaken in the literature to analyse the dead-time effect in PWM inverter, resulting in different modelling techniques of dead time. This helps in developing new and improved techniques for dead-time distortion compensation with or without current sensor. However, this requires almost accurate modelling of the system, from which self-tuning of the parameters may also become possible. Otherwise, the compensation will not be accurate, which may result in higher THD of inverter output voltage and current than that expected after executing compensation. Generally, inverter pole-current polarity is used to correct dead-time distortion. The presence of significant ripples at switching frequency near current-zero zone leads to several current zero-crossings, and the current polarity changes with each zero clamping. This makes conventional dead-time distortion correction methods unsuitable for such cases. A new method for compensating dead-time effect has been presented in Ben-Brahim et al. (1998), which also overcomes the ‘zero-current clamping’ problem. In this proposed method, near the current-zero-zone, a ‘smooth hysteresis’ band depending on current ripple is used for the compensation. The width of this band is presented as a function of current ripple. Hence, the current distortion at the zero-current clamping area is reduced. Chierchie et al. (2014) discussed the dead-time effect on the PWM spectrum for arbitrary but periodic modulation signals. As reported in this paper, dead-time distortion brings down the quality of the output voltage signal by introducing lower-order harmonics. The paper also discusses that even very small dead time causes high distortion as compared to that resulting from non-modelled distortion sources of the inverter e.g. switch and diode voltage drops. The paper also introduces a distortion-index based design tool, which aids in the selection of carrier frequency or dead time according to a certain distortion level. A compensation method capable of self-tuning to

the inverter and load properties has been proposed in Cichowski and Nieznanski (2005). This is based on current distortion minimisation. The reflection of the harmonic distortion of the output voltage is clearly observed in the output currents, and thus a compensation scheme for reducing the voltage distortion can be tuned based on current distortion minimisation. The calculation of the harmonics is carried out with a simple recursive DFT algorithm. The distortion indicator is averaged and applied to the search algorithm.

Using a detailed physical model for the inverter, Bedetti et al. (2015) presented a piecewise compensation technique. Here, a new self-commissioning identification procedure is involved, which utilises multiple linear regression (MLR). MLR is used at high current and straight line regression is used at low current for better curve fitting for distortion and resistance voltage. This finally provides a higher accuracy in the inverter nonlinear compensation. However, some parasitic parameters varying with circuit state are approximated, resultant to which the compensation accuracy is reduced in offline methods. In Ye et al. (2022), an accurate harmonic calculation model for the SPWM in unipolar mode has been developed for accurate analysis of the dead-time effect. This model is used to generate the compensation waveforms, and then these are added to the sinusoidal reference voltage. The proposed method considers the phase delay of the fundamental voltage owing to dead time and requires no additional hardware for current polarity detection. Hence, the performance of this compensation technique is not affected by the current ripple and current zero-clamping. Also, the technique can be easily implemented in a digital controller. In Wang et al. (2022), a comparative study of the dead-time distortion in continuous and discontinuous PWM techniques has been given. Here, an improved PWM technique is presented to reduce dead-time distortion, where the compensation signals are added to the modulation signals to reconstruct the dead-time voltage error. The zero-sequence signal injection technique and average current control technique are discussed in this article. This scheme only involves simple addition and subtraction, and can be easily implemented in digital signal processors (DSPs).

In some compensation strategies, the switching pulses are directly taken and switching interval error is calculated therefrom. This can help in compensating the dead time directly e.g. by addition of the compensated switching time or by adjustment of the switching frequency etc. In some techniques, the algorithm is developed in such a way that dead time is introduced without having its distortion effect. Some of the techniques have been developed in such a way as to eliminate the need for direct application of dead time. Oliveira et al. (2007) proposed a compensation technique, where the switching frequency is adjusted according to the modulating waveform amplitude for avoiding unfeasible pulse widths of gating signals and also for minimising the THD of the inverter output voltage. However, the calculation and algorithm become complicated owing to the variable frequency. It also requires an additional hardware and considerable amount of effort to determine the stable parameter set. The best results are obtained in the high-frequency range. Lee and Ahn (2014) directly compensate the switching interval error of the effective voltage vectors due to dead time. The average output voltages for each phase can be determined from the practical switching voltages within the switching intervals for a sampling period, and thereafter the error between the average output voltage and voltage command for each phase is determined. The practical switching interval error of each phase can be compensated by the addition of the compensated switching time, where a simple circuit is involved in current polarity detection. However, this technique may require extra hardware or complicated signal processing algorithms. In Weerakoon et al. (2016), at a time, depending on current polarity, the dead time is added to the rising edges of the gate drive signal of one device in an inverter leg, whereas the falling edges are advanced by the time equal to dead time. The gate drive signal of the other device of the same leg is kept unaltered. This adds the required dead time. The method results in accurate inverter output voltage without any magnitude or phase errors. This leads to a very simple procedure which is, however, not accurate for low currents. A novel hybrid space-vector-based dead-time compensation method of SVPWM has been proposed in Mao et al. (2011), which achieves the compensation through changing the traditional 180° turn-on mode into a 120°-plus-180° turn-on mode. Thus, as depicted in Figure 30, an inverter leg can have three possible states, whose values are ‘1’ (when only the upper switch for that leg is ON), ‘0’ (when only the lower switch for the leg is ON), and ‘φ’ (when both switches of the inverter leg are OFF). Since there are finite intervals, where both switches of the same inverter leg will remain OFF, insertion of dead time is no longer required, thereby eliminating dead-time distortion. However, this model suffers from a slight reduction in inverter gain.

In several research works, different controllers have been designed and used e.g. predictive current controller (PCC), repetitive controller (RC), proportional-resonant (PR) controller etc. for dead-time distortion compensation. These controllers may utilise the distortion model or adaptive techniques and in some cases compensate the fundamental and sixth harmonic components of the distortions of the output voltage. However, some of the

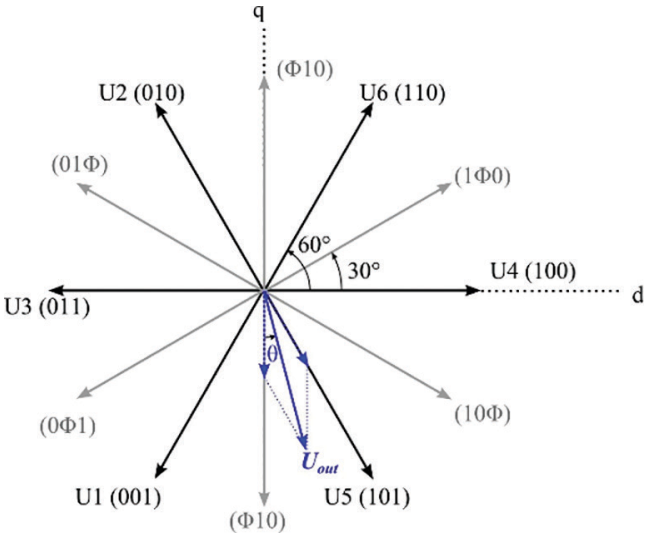


Fig. 30. Hybrid vectors sequence schematic (Mao et al., 2011).

techniques are suitable for slow dynamic applications, whereas some of these suffer from increased cost and complexity of implementation. Kim and Park (2007) compensate the fundamental and sixth harmonic components of the distortions in the inverter output voltage that are due to the dead-time effect in a synchronous reference frame. A feed-forward technique for the fundamental-frequency compensation and a feedback loop having current controllers for the harmonic compensation are combined. Here, the harmonic compensator having all-pass-based adaptive band-pass filter is developed. It builds up the feedback loop with current controllers for compensating the harmonic distortions due to dead-time effects. The technique does not depend on phase current polarity and nonlinear switching characteristics, varying with inverter operating conditions. However, additional hardware detection circuitry is required, increasing the cost and complexity. In Herran et al. (2013), a closed-loop compensation technique using a PCC for grid-connected PWM VSI of a single-stage PV system has been developed, where observer parameters can be adaptively tuned. A nonlinear disturbance model is involved for developing a feed-forward compensation signal, which eliminates the current distortion due to zero-current clamping effect. Here, a new closed-loop adaptive adjustment technique is presented to enable real-time fine tuning of the compensation model parameters. This improves the accuracy of this technique under varying physical conditions. The algorithm is computationally efficient and its implementation is straightforward and can be added to an existent PCC to improve its dead-time compensation capability without any change in its internal structure. However, this technique is suitable only for slow transient applications and is not applicable to different working conditions. A steady-state high-performance VSI nonlinearity compensation technique using a PCC approach has been presented in Abronzini et al. (2016). Here, a step-by-step voltage compensation is achieved based on the current error, calculated within each control interval. The switching pattern is time-shifted properly for each modulation time for reducing the effect of nonlinearity on the current ripple. This results in a complete compensation within a whole fundamental period. To overcome the zero-current clamping effect, the proposed compensation method is implemented in a recursive way. However, this technique is suitable only for slow dynamic applications. Yang et al. (2018) proposed a compensation technique involving a RC and finite impulse response (FIR) filters. This technique does not require any hardware modifications and can be implemented in a low-cost digital controller. Here, the PR controller is taken as the fundamental-frequency current controller for ensuring a fast tracking of the fundamental grid current, whereas the RC is taken as a plug-in parallel harmonic compensator. However, the complex algorithm requires a large amount of memory.

Continuous research is also going on to develop new current-sensor-less dead-time distortion compensation techniques. These techniques may compensate the distortion by comparing the actual duty cycle with the ideal one or derive the current polarity indirectly from other signals available. These strategies can reduce the cost of the current sensor or eliminate the problem of current measurement error. A fully digital algorithm that compares the actual duty cycle (measured at the power stage) with the ideal one has been proposed in Chierchie and Paolini

(2017). Comparing pulse widths instead of comparing the amplitude of the demodulated PWM signal results in the emergence of error. Dead-time distortion shaping strategies are developed for displacing the distortion spectra far away from the frequency band of interest. The presented technique has a low computational complexity, which requires only a few additions and multiplications. It also need not require inverter-current sensing, which overcomes the problem of current measurement error arising from noise and current ripple. A new current-detection-independent compensation technique has been proposed in Liu et al. (2017). This works on terminal voltage A/D conversion, from which both the compensation time and the current polarity can be extracted. The technique is centred around the compensation time T_c, which is defined as the error between the ideal and the actual terminal voltage duration in one switching period. The paper demonstrates how the current polarity can be determined from compensation time and also from the amplitude of terminal voltage sampled at a certain instant. The presented technique has the potential for achieving significant improvements in terms of the performance of the fixed, online, and even feedback compensation. However, here an accurate dead-time voltage error model is required, considering different switching modes caused by the inductor current ripple. Shen and Jiang (2019) discussed a novel compensation technique that can reduce the effect of the current ripple and improve the accuracy of dead-time compensation. The proposed technique derives the current ripple in real time, from which the phase-leg currents' actual trajectory can be reconstructed. This can then predict their peak values according to rising and falling edges for PWM signals. Thus, the accuracy can be improved by implementing the compensation depending on the relevant instantaneous switching current direction. The technique is extended for implementing dead-time compensation in inverters, based on the instantaneous direction of switching current.

The above study reveals that dead-time distortion is inherently present in all PWM-inverter-based systems, and unless a dedicated compensation scheme is kept in place, this will cause serious distortion in output voltage and current. This may often render the output voltage and current unacceptable as per existing standards (e.g. IEEE 519-2014). Various techniques have been developed to compensate for the dead-time distortion. However, these techniques either increase the complexity of PWM generation, or the system complexity, or both. Hence, the search is still on to mitigate this problem, using minimal resources, while not compromising on the accuracy of the compensation.

A summary of the important results from the various major PWM techniques, in percentage form, has been presented in Table 1. This table brings out a comparative evaluation, based on numerical values, between the various major techniques, and highlights their advantages and shortcomings.

The table clearly shows that the amplitude of the fundamental component of the inverter output voltage increases as shifted from SPWM technique to SVPWM technique in a linear operating region. This amplitude again increases when entered into the over-modulation region, achieving its highest value in over-modulation region-II. Though the amplitude of the fundamental component of the output voltage of the inverter increases in SVPWM as compared to SPWM, the THD also increases in SVPWM in all the operating regions. This effect becomes more pronounced in over-modulation-II region in SVPWM. With the introduction of dead time, the THD increases more, deteriorating the voltage profile. The fundamental component of the output voltage also decreases with introduction of dead time. The CMV of the inverter in SVPWM technique is larger than that in SPWM technique and its value becomes highest for SVPWM technique in over-modulation-II region of operation. It is also to be noted that the attendant increase in the CMV corresponding to the case of dead-time introduction is greater than that not associated with any dead time.

With/without dead time	PWM strategy	Amplitude of fundamental component of line voltage w.r.t DC-bus voltage (%)	Percentage THD of line voltage	RMS value of CMV w.r.t DC-bus voltage (%)
Without dead time	SPWM in linear operating zone	82.27	1.12	0.01
	SVPWM in linear operating zone	95.02	1.22	8.06
	SVPWM in over-modulation operating zone-I	99.67	3.37	8.45
	SVPWM in over-modulation operating zone-II	104.9	4.25	9.22
With dead time	SPWM in linear operating zone	79.24	1.87	7.74
	SVPWM in linear operating zone	92.07	1.96	8.74
	SVPWM in over-modulation operating zone-I	97.96	3.91	9.04
	SVPWM in over-modulation operating zone-II	104.92	4.86	9.26

Table 1. Summary of different performance parameters for the SPWM and SVPWM techniques.

3. Future Scope

This paper has focussed on a few selected problem areas related to two-level PWM VSI, and reviewed research works relevant to these areas. The underlying principles, advantages, and shortcomings of such solutions have been discussed in this paper. It may be noted that the problem areas as discussed in this paper are not entirely independent but often interrelated. Hence, a solution that leads to improved performance in one area often results in deteriorated performance in other areas. Based on the above, this paper proposes a few directions in which future research work can progress. These are mentioned in the following subsections.

3.1. Improving overall gain and harmonic content in the linear and over-modulation zones

Several researches have been conducted over the past few decades and in recent years for improving the overall gain of the inverter with proper utilisation of the inverter DC bus and maintaining the harmonic content within a certain limit. For a three-phase PWM inverter operating on SPWM strategy, the gain value stands at 0.612. For third-harmonic injected SPWM, as well as SVPWM strategies in the linear zone, this value can be pushed to about (0.612 × 1.15) = 0.7. However, practical PWM inverters have a lower value of maximum achievable gain. This is due to two primary reasons:

(i) Loss of pulse width owing to dead time
(ii) Limitation of minimum pulse-width requirement

Thus, one prospective direction of research may be to formulate improved PWM techniques, by which the gain can be pushed to higher levels in the linear and over-modulation zones, while maintaining a low harmonic content in output voltage and gain-linearity. This may be made possible by implementing advanced control algorithms in high-level digital signal controllers. New control techniques, e.g. modulated model predictive control (Schuetz et al., 2023), can also be developed, which can be represented as a single optimisation problem by combining control and modulation. This can generate the optimum duty cycles for modulation. It is to be ensured that such algorithm can easily be implemented without increasing computational burden and that it would result in good steady-state and transient performances, even with parametric uncertainties and variations.

3.2. Reduction of common-mode signal

Another aspect of PWM inverters, namely CMV and its reduction, has also been discussed in this paper. Such CMVs are unwanted as they cause CMCs to flow through motor bearing or body capacitance, thereby reducing their lives. Several attempts have been made to reduce such CMV. However, such strategies may lead to other problems, such as the reduction of the DC-bus utilisation (i.e. lower inverter gain), increased switching loss, more complex control algorithm etc. Thus, another prospective research area can be to formulate efficient PWM strategies to reduce or eliminate the CMV, while maintaining satisfactory performance levels on all other fronts. Different techniques can be developed, depending on how the ZVVs can be replaced by synthesised voltage vectors (SVVs) obtained from adjacent active vectors (Parvathy and Kumar, 2023). New methods are also being attempted that can replace the zero vectors generated from CMV spikes during inverter commutation (Deng et al., 2023).

3.3. Reduction of dead-time distortion

Presence of dead time increases the THD of the output waveform, as well as brings down the amplitude of the fundamental. Extensive research has been carried out over the past few decades to eliminate/reduce this distortion. However, these different techniques have different limitations, such as increase of complexity of structure and efficiency reduction owing to topology change with introduction of additional switches, multiple zero-cross detection problem owing to ripple in current, increase of complex control and additional control hardware, separate dead-time compensation block etc. Hence, a prospective research direction may be the development of PWM strategies and/or inverter topologies having the potential to overcome the dead-time distortion problem without encountering increased complexities. One such area is related to dead-time distortion compensation with reduced sensor count, which automatically results in less cost and complexity of the set-up. Another approach is to develop a current-controlled VSI, which also includes the switching delay time and switch voltage drop compensation, along with dead-time distortion compensation (Yamamoto et al., 2020).

The authors of this paper are also concentrating on the area of applying one-cycle control (OCC) technique for dead-time distortion compensation in PWM VSI (Chatterjee et al., 2022).

4. Conclusion

This paper has presented a review on selected areas of two-level PWM-controlled inverters. The scope of the review is focussed on the areas of (a) the utilisation of the DC bus, (b) switching-loss reduction, (c) CMV reduction, and (d) dead-time distortion compensation. Extensive survey has been presented in these areas. The present article also briefly discusses the working principles, as well as the advantages and shortcomings, of the various approaches adopted in the studies cited herein. Some elementary simulation results are also presented, which demonstrate some of the above limitations characterising the performance of two-level PWM inverter in general form. Finally, the paper points to some prospective directions in these areas, in which research may continue in the immediate future.

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Appendix

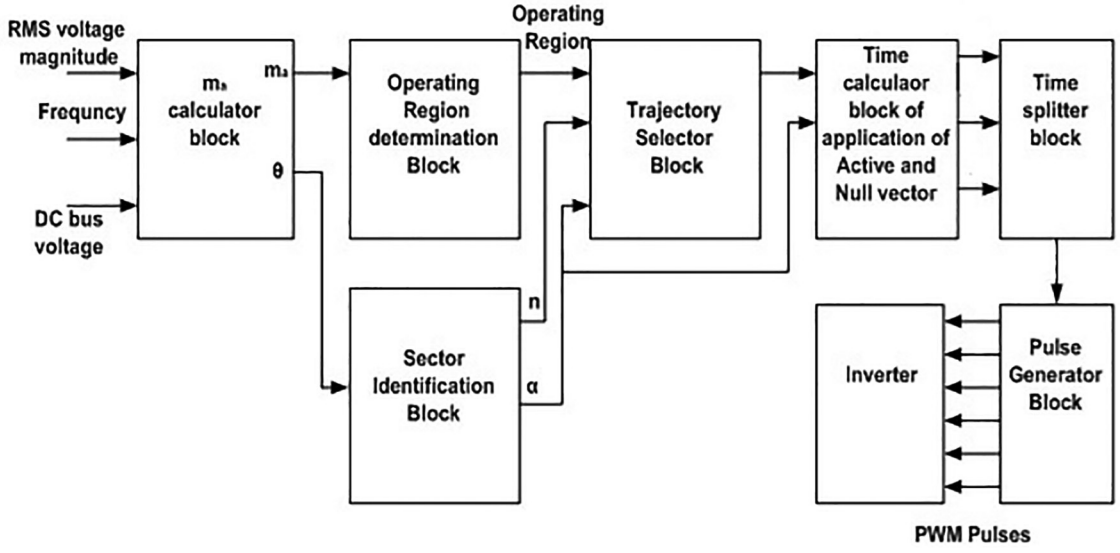

Fig. A1. Block diagram representation of the structure of simulation program for SVPWM.